Increasing electrical conductivity in sputter-deposited Si/SiGe multilayers through electrical pulse based annealing

P. Pichanusakorn, N.B. Elsner and P.R. Bandaru

Low temperature deposition, by sputtering, on flexible/plastic substrates offers a relatively cheap alternative for fabricating single-/multilayer thin film devices. However, sputtering yields amorphous material, with low electrical conductivity, and requires subsequent annealing. Demonstrated is a new method of crystallisation, where controlled application of electrical pulses to sputter deposited Si/$Si_{0.8}Ge_{0.2}$ multilayers is shown to decrease the electrical resistance by as much as 80%.

Introduction: Commercially viable multilayer thin film Si/SiGe deposition processes such as sputtering, which can be used widely for electronic and photonic devices [1, 2], yield amorphous material of poor crystalline quality and low electrical conductivity. Currently used methods to improve conductivity, such as furnace and laser annealing, are inadequate for multilayers and also unsuitable for organic/plastic substrates.

It has been shown, for example, that amorphous Silicon (a-Si) can be crystallised through furnace heating if the temperature is raised to at least 873 K [3]. This crystallisation temperature (T_{cr}) can be lowered if the Si is alloyed with Ge, e.g. for a-$Si_{0.8}Ge_{0.2}$, T_{cr} is ~823 K [3]. Keeping these limitations in view, we propose that Joule heating of the layers could provide an alternative method for crystallisation. In our method, electrical currents, in pulse form, were injected into the sputter deposited multilayer structure and the consequent Joule heating utilised for crystallisation. The electrical pulse amplitude and duration were tuned for preferential annealing and substrate insensitivity. Initial results of crystallisation in a-Si/a-$Si_{0.8}Ge_{0.2}$ multilayer structure on organic substrates, through electrical measurements, are presented.

Experiment: The Si/SiGe multilayer samples used in this investigation were fabricated on Kapton substrates via sputtering of *n*-type Si, and *n*-type $Si_{0.8}Ge_{0.2}$ alloy targets, in an Argon gas ambient. A thick, 200 nm Si buffer layer was first deposited, followed by 400 alternating layers each of $Si_{0.8}Ge_{0.2}$ and Si, with individual layer thicknesses of ~10 nm. Electrical contacts were made via Ti (10 nm)/Al (150 nm) pads deposited through e-beam evaporation. The experimental setup for applying current pulses to the sample is shown in Fig. 1. A constant voltage pulse (from a Keithley 2400 source meter) was applied to the sample. At the maximum voltage level of 210 V, the source meter can supply 105 mA of current, which corresponds to a maximum power ($\boldsymbol{P}$) output of ~22 W, with a 2 kΩ load resistor (R_L) – inserted in series to limit the heating power to the sample. The supply voltage, V_o, and voltage drop over the series resistor, V_r, were monitored through a digital oscilloscope (TEK2024 – 200 MHz bandwidth, 2 GS/s sampling rate, using two channels: ch1 and ch2). The resistance of the sample, $R_s = [V_o - V_r/V_r]R_L$, was subject to a heating power ($\boldsymbol{P_s}$), of $P_s = R_s[V_o/R_s + R_L]^2$, which is maximised when, $dP_s/dR_L = 0$ and $R_s = R_L$. Given that V_o has the nominal value of 210 V, the maximum power on the sample was, $P_{s,\max} = R_L[210/2R_L]^2 = 11,025/R_L$.

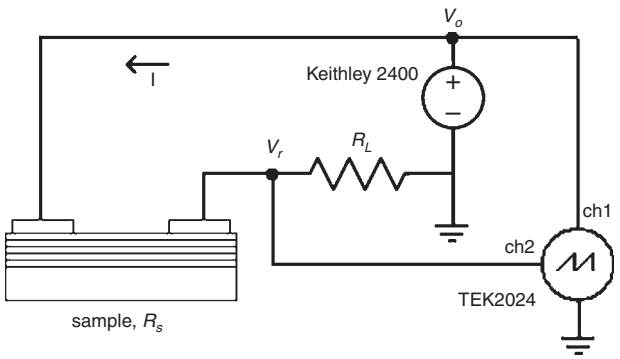

Fig. 1 *Layout for electrical pulse induced annealing of sputter deposited Si/$Si_{0.8}Ge_{0.2}$ multilayer structures*

Pulses, optimised in amplitude and duration, derived from source meter (Keithley 2400) were used to induce Joule heating and lower the sample resistance (R_s). A load resistor (R_L) placed in series controls maximum power applied to sample.

Results and discussion: The temperature of the sample during pulse application was estimated through resistance measurement. *In situ* resistance was monitored on a number of samples as they were heated from ~300 to 673 K at a rate of 10 K/min in an evacuated tube furnace. The ambient temperature was measured with a K-type thermocouple placed close to the sample. The sample resistance, $R(T)$, decreases with temperature, typical of a semiconductor, and was fit to, $R(T) = R_0 \exp(E_a/k_B T)$, where E_a is the activation energy (eV), k_B the Boltzmann's constant (~86 μeV/K), and T the temperature (K). This fit, however, would only account for the reversible change in resistance, and is applicable only in the 300–823 K range, after which crystallisation is initiated. Then, the crystallisation of a-Si (or silicon rich, a-$Si_{0.8}Ge_{0.2}$) would irreversibly decrease the electrical resistance, by as much as four orders of magnitude [4, 5], and the activated model is inapplicable. An E_a of 0.25 eV was determined from the slope of data in Fig. 2. The temperature (T) was then estimated through: $T = 0.25/k_B \ln[R(T)/R_0]$.

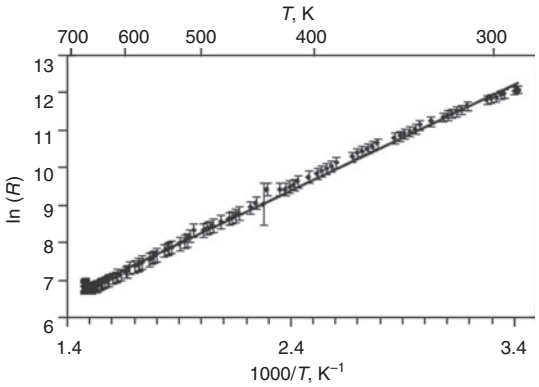

Fig. 2 *Change of electrical resistance with temperature, for multilayer samples yields, from the slope, an activation energy (E_a) of 0.25 eV (such a calibration used for monitoring approximate sample temperature)*

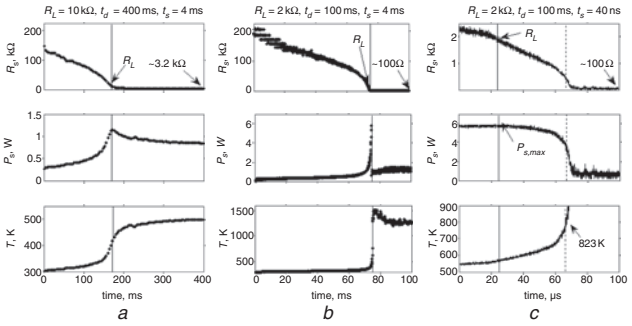

Fig. 3 *Variation of sample resistance (R_s), heating power (P_s), and temperature (T) with time, during electrical pulse application on three distinct Si/$Si_{0.8}Ge_{0.2}$ multilayer samples*

Solid vertical line marks point where $R_s = R_L$ (load resistance), for maximal heating power. R_L, pulse duration (t_d) and sampling time (t_s) indicated at top of each Figure

a Small $P_{s,max}$ (~1.1 W): no permanent reduction in R_s

b Large $P_{s,max}$ (~5.5 W): irreversible reduction in R_s, possibility of sample crystallisation

c Higher resolution sampling of $P_{s,max}$. Dotted line near $T = 823$ K could correspond to onset of crystallisation

We then examined the effect of electrical pulse application and the consequent role of Joule heating on the electrical resistance of the Si/SiGe multilayer structure. In Fig. 3*a*, a test sample was subjected to a single 400 ms long electrical pulse with the maximum power, $P_{s,max}$, limited to ~1.1 W by a 10 kΩ load resistance, R_L. The sample resistance, R_s, decreased owing to the Joule heating as expected. The heating power (P_s) was dependent on R_s, and was maximised when $R_s \sim R_L$ (indicated by the vertical solid line in the Figure). The temperature-time plot showed the consistency in the variation of P_s and the estimated temperature, i.e. the temperature changed most rapidly when P_s approaches $P_{s,max}$ and levels off as P_s decreases afterwards. At 1.1 W, the heating rate was modelled to be as high as 3500 K/s compared to a typical 50 K/s heating rate in a rapid thermal annealing (RTA) oven. We also observed that owing to the Joule heating, R_s has been reduced to ~3.2 kΩ during the electrical pulse application, while the corresponding

sample temperature increased to ~500 K. Successive experiments with other values of R_L showed that the final temperature and the overall heating rate was higher for larger values of $P_{s,max}$ which can then be used as a relevant experimental parameter. In line with the goal of inducing crystallisation, and increasing the electrical conductivity, one would wish to maximise $P_{s,max}$. Generally, a larger $P_{s,max}$ would be expected for multilayered structures with a larger number of layers and/or smaller concentration of Ge in the $Si_{1-x}Ge_x$ layers.

In heating processes characterised by smaller $P_{s,max}$ (as in Fig. 3*a*), the maximum temperature of the sample was still below the T_{cr} of 820–870 K. Consequently, the decrease in R_s was due solely to change in temperature, and was reversible, i.e. after the electrical pulses were terminated and the sample was cooled, R_s returned to its original value. In such a scenario, the equation used to determine the temperature is valid. For a larger $P_{s,max}$ (~5.5 W as in Figs 3*b* and *c*), the resistance change observed in the sample could be due to the combined influence of purely temperature induced reversible change and crystallisation induced irreversible change. It was noted that the temperature determination, employing an activated model, may not be accurate for the case of crystallisation induced resistance change. However, we do observe a large permanent decrease in the sample resistance subsequent to pulse application (from 200 to 0.1 kΩ), indicating an amorphous to crystalline phase transformation of the sputter deposited multilayer films. From this, we can be confident that the sample temperature does exceed T_{cr}. The threshold value of $P_{s,max}$ for the permanent resistance reduction was seen to be ~4 W. It is noted that Fig. 3*c*, obtained by monitoring the sample resistance change at much higher (10 ns) resolution, was obtained only for 100 μs near the point of maximum power as the amount of data was limited by the oscilloscope buffer size. Generally, a decrease in resistance of up to 80% was observed for a large number of samples, subjected to the pulse treatment. While the quality of the surface was not examined in detail, it was seen that the Kapton substrate was not visibly affected by the pulses and maintains its integrity.

Conclusions: Our initial results are promising and provide proof of the principle that controlled electrical pulse based heating/annealing could be used to increase the crystalline character in sputter deposited Si/SiGe multilayer samples and enhance electrical conductivity. To ensure high overall heating rate with minimal substrate damage the electrical pulse (amplitude and duration) could be optimised such that the target temperature (corresponding to T_{cr}) is reached and the pulse terminated as soon as the $P_{s,max}$ is reached.

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P. Pichanusakorn and P.R. Bandaru (*Department of Mechanical and Aerospace Engineering, Materials Science Program, UC, San Diego, La Jolla, CA 92093-0411, USA*)

E-mail: pbandaru@ucsd.edu

N.B. Elsner (*Hi-Z Technology, Inc., 7606 Miramar Road, San Diego, CA 92126-4210, USA*)

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