

In-Plane Thermal Conductivity Determination in Silicon on Insulator (SOI) structures through Thermoreflectance measurements

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ABSTRACT

Heat dissipation in Silicon-On-Insulator (SOI) based microdevices is hindered in the silicon device layer by the low thermal conductivity of the neighboring oxide and reduced in-plane thermal conductivity in very thin layers. This work shows that the in-plane thermal conductivity of a 260 nm thick device layers in SOI substrates can be characterized by measuring the temperature distributions induced by AC joule heating through microfabricated heaters by a scanning thermoreflectance technique. These data were fitted to numerical solutions of the heat conduction equation calculated using COMSOL® Multiphysics modeling software, suggesting the in-plane thermal conductivity of the device layer is reduced to $90 \pm 10 \text{ W/(m.K)}$, which is consistent with phonon boundary scattering theory predictions.

INTRODUCTION

Silicon-On-Insulator (SOI) wafers are widely utilized in microdevice fabrication for the advantages offered by the electrical insulation of the device layer from the substrate, allowing for smaller parasitic capacitances, higher device density, and reduced power requirements. Heat dissipation is a central issue to the performance of these devices, which is significantly hindered by low thermal conductivity of the buried oxide and possibly reduced in-plane thermal conductivity in very thin single-crystal silicon device layers [1]. Modeling of thermal conductivity of silicon is typically done by solving the Boltzmann Transport Equation (BTE) for acoustic phonons; thermal energy stored by optical phonons is primarily capacitive and does not significantly contribute to heat conduction due to small phonon group velocity [2]. As phonon-boundary scattering has been identified to be the primary mechanism by which thermal conductivity is reduced in two-dimensional structures, the BTE was modified to include an additional boundary scattering term for thin films [3]. Single-crystal silicon thin films and SOI based substrates have been extensively measured and modeled within this framework [4-9]. In this study, we demonstrate an experimental method for the determination in-plane thermal conductivity of the device layer in SOI substrates using scanning thermoreflectance. Numerical solutions of the Fourier Heat Conduction Equation obtained with COMSOL® are fit to experimental thermal profiles, implying a reduction in the thermal conductivity of the device layer consistent with BTE models.

Thermoreflectance thermometry is a differential optical technique which monitors a relative change in reflectance in a conducting material that is proportional to the thermal variation of the sample. In semiconductors, the complex index of refraction varies as a function of temperature which results in a temperature dependent reflectance value. This modulation is due to the sensitivity of the absorptive component of the dielectric constant on thermally induced shifting of the band gap and the Fermi energy with respect to critical points in the density of states. For

small temperature perturbations, the relation between the change in temperature and the normalized reflectance can be described by the linear relation

$$\frac{\Delta R}{R} = \left(\frac{1}{R} \frac{\partial R}{\partial T} \right) \Delta T = C_{Th} \Delta T, \quad (1)$$

where R is the reflectance, T is the temperature, and C_{Th} is the coefficient of thermoreflectance which generally falls in the range of 10^{-3} and 10^{-4} 1/K for semiconductors. While C_{Th} can be calculated for a given material and wavelength of incident light, it is highly sensitive to surface quality and presence of transparent overlayers [10]. In practice, the C_{Th} is found experimentally by simultaneously monitoring the change in reflectance and temperature using an additional technique, such as a thermocouple. Knowing the absolute temperature profile is unnecessary in this study, as the relative change of the calculated temperature profile as a function of distance from the heater is used to fit the data, not the absolute temperature profile. Thus, all data will be listed in arbitrary units of temperature, proportional to the measured $\frac{\Delta R}{R}$ value.

EXPERIMENTAL DETAILS

Thermoreflectance is performed in the visible light regime affording superior spatial resolution in comparison to other thermal profiling techniques, such as infrared imaging [11]. Point scans rastered across a sample surface yield a high signal to noise ratio, while large areas can be quickly imaged using a photodiode array [12] or charge-coupled device (CCD) camera [13] in conjunction with special detection and signal processing schemes. The experimental setup performed in this study used point scans with a 10 mW, He-Ne, 632.8 nm laser source which was focused by a 36x, N.A. 0.5, Ealing reflecting objective lens yielding a spot size on the order of 2 μ m. The Device Under Test (DUT) consists of an SOI substrate, with a device layer 260 \pm 15 nm thick, a buried oxide layer 1 \pm 0.05 μ m thick and a handle that is 675 μ m thick. The device layer is lightly p-doped, with an electrical conductivity of 14-22 Ω .cm. Ti/Au contacts were microfabricated on the SOI surface and used as resistive heaters to obtain thermal profiles. The heater thickness was 200 nm, with widths of 5 μ m, 34 μ m, and 90 μ m to evaluate the effect of heater width on thermal transport through the device layer. It is hypothesized that wide heaters will deliver a higher proportion of thermal energy perpendicular to the surface into the substrate in the limit of 1D heating for an infinitely wide heater. Conversely, narrow heaters will act more like a point source, increasing the temperature peak near the heater edge associated with the heat trapped in the device layer. To evaluate the possible need for an electrical insulator between the heater and the substrate, a 30 nm silicon dioxide was sputtered before the heater was deposited on otherwise identical samples for comparison.

To obtain thermal profiles, the sample was heated by the electrodes subjected to an AC electrical current at frequency $f=2677$ Hz. The power dissipated due to Joule heating is proportional to the current squared, which equilibrates to a DC increase in the sample temperature summed with a sinusoidal fluctuation of the temperature at frequency $2\omega=2*2\pi f$; the thermoreflectance signal acquired by a p/i/n diode detector is measured by a lock-in amplifier, referenced to the second harmonic of the heating current. Using this method, only the AC thermal wave is measured as it propagates through the substrate, not the steady-state thermal profile.

The measurement of thermal profiles generated by transient heating is accurate under a wide array of conditions, with respect to steady-state [14]. By operating at heating cycles much shorter than the thermal time constant of the DUT, which is on the order of minutes, error introduced by convection can be ignored. In addition, while operating at room temperature and when joule heating is small, the error due to radiation is negligible. The real part of the thermal penetration depth, $1/q$, of the thermal wave generated by heating current frequency ω is defined as, $\text{Re}\left[\frac{1}{q}\right] = \sqrt{\frac{2D}{(2\omega)^2}}$, where D is the diffusivity of the material. Choosing the correct ω will preclude the need to consider thermal interactions between the DUT and the sample holder. As scanning thermoreflectance is a non-contact, optical method, it offers advantages over traditional resistor-based measurements in that it can accommodate unique sample geometries and contains fewer sources of thermal capacitances typically introduced by thermal probes.

DISCUSSION

A plot of the temperature with respect to distance from the heater edge of the SOI samples, with and without a silicon dioxide insulating layer separating the heater and substrate, is shown in figure 1. The curves have a characteristic shape with a sharp decay in temperature near the heater edge associated with heat trapped in the device and buried oxide layers. The tail of the thermal profile is generated from the remaining heat that has dissipated into the silicon substrate.

Juxtaposing the two sets of data suggests the reproducibility of these measurements and insensitivity of the lateral heat transfer to thermal boundary resistances that may exist between the heater and the substrate. Since the C_{Th} of each sample is unknown, we cannot confirm that absolute temperature profiles are the same from a single heating stimulus. However, in the plot, one curve has been scaled by a constant to match the other and since the shapes are nearly identical, very similar in-plane thermal transport can be assumed. The similarity in the plots also verifies that there is no need for an electrically insulating layer beneath the heater, which seems to be a common practice in experiments that use on-ship Joule heating, e.g. 3ω method, even on substrates that are many orders of magnitude less conducting.

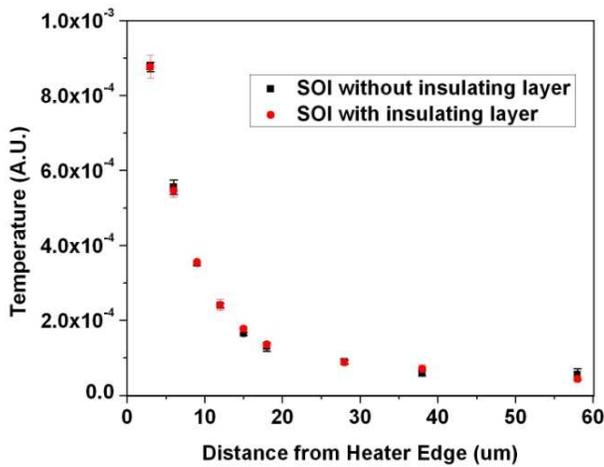


Figure 1. The scaled thermal profiles of the SOI with 260 nm silicon device layer thickness, with and without a silicon dioxide layer insulating the heater from the substrate.

To determine the in-plane thermal conductivity of the device layer, a 2D numerical model was used to solve for the time dependent thermal profile of the cross section of the SOI/heater sample. The 2D modeling is adequate this case due to the large heater length (1 mm) in comparison to the thermal penetration depth in silicon ($1/q=73 \mu m$). The thermal conductivity values used in the handle and buried oxide layers correspond to bulk values, $k_{Si}=142 W/(m.K)$ and $k_{SiO_2}=1.3 W/(m.K)$, while the thermal conductivity of the device layer remains a free variable. Because the heating method is transient and at room temperature, heat transfer by convection and radiation with the surrounding environment was neglected. Setting the boundary condition of the bottom of the substrate to a fixed temperature had little effect on the resulting heating curves and was then considered to be an insulating boundary. Thermal boundary conductance spanning experimental values found for most intimate solid/solid interfaces, $10^7-10^8 W/(m^2.K)$, were used [15]. However, the in-plane thermal profile did not change between the extremes of this range. The thermal power generated by the heater was approximated by I^2R resistive heating.

The measured thermal profile of the sample is displayed concurrently with calculated thermal profiles of varying device layer thermal conductivity in figure 2. It should be noted that the calculated profiles have differing peak temperatures for a given heating input. The C_{Th} of the sample has not been determined, hence, each calculated curve is scaled to have identical peak values to provide comparison for best-fit evaluation, as shown in the plot. In other words, the fitting process is based on the relative shape of the curve but not the absolute values of the temperature profile. Since the sample is semitransparent and contains multiple layers, the measured thermal data is a linear combination of the thermoreflectance signal from the device layer and the substrate. Accordingly, the calculated thermal profile is a weighted sum of the heat fluctuations in these two layers. For the 260 nm thick sample, the device layer and handle are weighted equally. The buried oxide is neglected as it is electrically insulating and does not produce a measurable thermoreflectance signal as it is electrically insulating. According to the fit, the device layer has a reduced thermal conductivity of $90 \pm 10 W/m.K$.

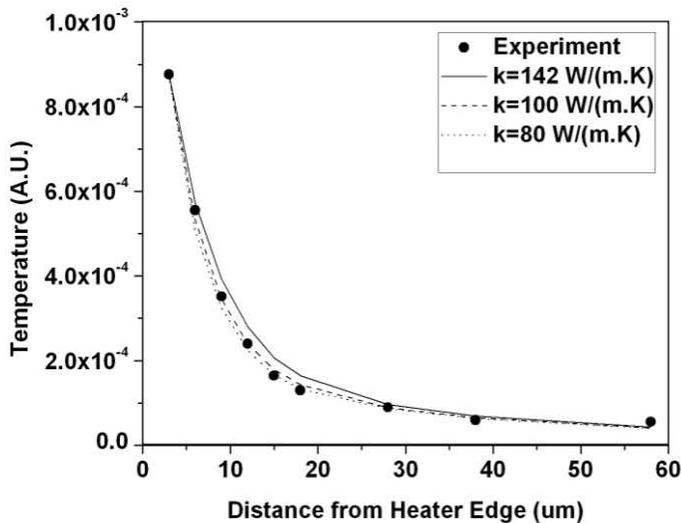


Figure 2. Plots of the experimentally measured thermal profile and calculated thermal profiles corresponding to device layer thermal conductivities equal to the bulk value, 100, and 80 W/m.K. The lowest two thermal conductivity values provide a range for the best-fit of the data.

The reduction of thermal conductivity in thin layers due to phonon boundary scattering has been formulated by Sondheimer by solving the BTE for phonons using the boundary conditions of a thin film [3]. The reduced thermal conductivity is equal to

$$\frac{k}{k_0} = \frac{1}{\delta} - \frac{3}{2\delta^2} (1-p) \int_1^{\infty} \left(\frac{1}{t^3} - \frac{1}{t^5} \right) \frac{1 - \exp(-\delta t)}{1 - (p)\exp(-\delta t)} dt, \quad (2)$$

where k/k_0 is the reduced thermal conductivity, δ is the ratio of the layer thickness, t , and the bulk phonon mean free path, l , and p is a parameter which describes the specularity of the reflection of phonons off the thin film surface, with $p=0$ corresponding to completely diffuse collisions.

The simplest way to estimate the average mean free path of phonons is to use the classical equation $k = \frac{1}{3} Cvl$, where C is the volumetric specific heat, and v is the velocity. This

expression has been shown to significantly underestimate the phonon mean free path when using bulk values because a significant contribution of the specific heat is derived from optical phonons which do not contribute to phonon conduction [16]. Instead, we have calculated an appropriate specific heat and weighted velocity for acoustic phonons from the experimentally determined dispersion relation of phonons in silicon [17]. The specific heat was derived as,

$$C_v = \frac{dE}{dT} = \frac{\hbar^2}{2\pi^2 T^2 k_B} \int \omega_{ph}^2 \exp\left(\frac{\hbar\omega_{ph}}{k_B T}\right) \left(\exp\left(\frac{\hbar\omega_{ph}}{k_B T}\right) - 1 \right)^{-2}, \quad (3)$$

where $\hbar = 1.602 \times 10^{-34} \text{ Js}$, $k_B = 1.38 \times 10^{-23} \text{ J/K}$, T is temperature, ω_{ph} is the phonon frequency, and b is the phonon wavevector. Solving this equation using the silicon dispersion relation, we find $C_{acoustic} = 9.47 \times 10^5 \text{ J/(m}^3 \cdot \text{K)}$ in comparison to the bulk value of $C_{bulk} = 1.63 \times 10^6 \text{ J/(m}^3 \cdot \text{K)}$. The weighted velocity was equal to an average of the longitudinal and transverse phonons scaled to the proportionality of their contribution to the specific heat, such that $v_{acoustic} = 2274 \text{ m/s}$, which is notably smaller than $v_{sound} = 6400 \text{ m/s}$. Assuming the bulk thermal conductivity value, we arrive at $l_{acoustic} = 202 \text{ nm}$. The specularity parameter p can be used as a fitting parameter in systems with very uniform interfaces. Within the SOI system, we assume diffuse reflection off the Si/SiO₂ interface due to silicon dioxide's amorphous structure and rough interface. We can also assume $p=0$ at the Si/air interface at the top of the device layer, evidenced by the near exact superposition of the curves in Figure 1. If specular reflection was significant in the sample without the top insulating layer, there would be a difference the thermal profile between the two samples.

Figure 3 shows the measured in-plane thermal conductivity in comparison with the theoretical thermal conductivity as a function of l and t . The reduced thermal conductivity is strongly dependent on the phonon mean free path, but is in fairly good agreement with the measured value. Experimental determination of the in-plane thermal conductivity of SOI with varying device layer thicknesses would further clarify the validity of our methods.

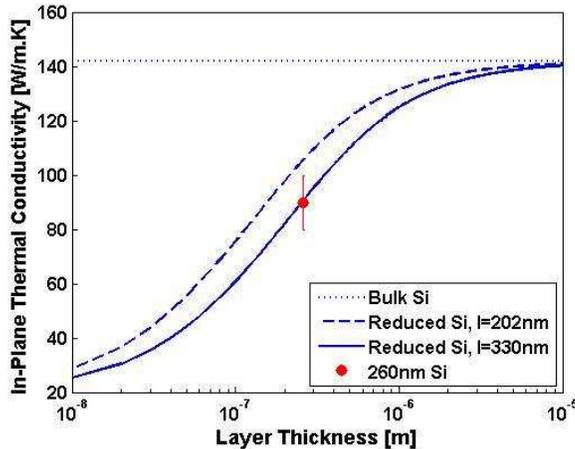


Figure 3. Plot of theoretical curves of bulk and reduced thin film silicon thermal conductivity, with measured value. Curves corresponding to the predicted and best fit mean free path are shown for comparison.

CONCLUSIONS

Our study shows that scanning thermoreflectance is a viable, non-contact method to determine the thermal characteristics of multilayer thin film structures, specifically the SOI system. We have experimentally shown a definitive thermal conductivity reduction in thin films and our results seem to be in good agreement with theoretical calculations. This technique also has potential for use in characterization of conducting thin films, or other nanostructures, on thermally insulating substrates.

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