Electronic and Photonic Applications of One-Dimensional Carbon and Silicon Nanostructures

Anupama B. Kaul

Jet Propulsion Laboratory, California Institute of Technology,
Pasadena, CA 91109

Ph: (818) 393-7186; Fax: (818) 393-6047

Email: Anupama.Kaul@jpl.nasa.gov

Prabhakar R. Bandaru

Jacobs School of Engineering, University of California-San Diego,
La Jolla, CA 92093-0411

Ph: (858) 534-5325; Fax: (858) 534-5698

Email: pbandaru@ucsd.edu

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TABLE OF CONTENTS

Section Page #

1.0 One-Dimensional (1D) Carbon Nanostructures for Complementary Metal-oxide-semiconductor (CMOS) Applications

2.0 Novel 1D Architectures for Electronics: Y-Junctions

3.0 Quasi-1D Graphene Nanoribbons

4.0 Suspended 1D Carbon Nanostructures for Nano-electro-mechanical-systems (NEMS) and Sensing

5.0 Silicon Nanowires (NWs) for Nanoelectronics and Nanophotonics

1.0 One-Dimensional (1D) Carbon Nanostructures for Complementary Metal-Oxide-Semiconductor (CMOS) Applications

1.1 Introduction and Overview

The semiconductor industry based on complementary metal-oxide-semiconductor (CMOS) Silicon (Si) transistors faces major obstacles to continued scaling according to Moore's law which is posing challenges in yielding high performance from increasingly miniaturized Si transistors. Such issues, which are highlighted in [**1**], include excessive leakage currents and high power dissipation from gate dielectrics that are just a few nanometers (nm) in thickness, as well as source-drain channel lengths approaching 10 nm or less. New materials and technologies are thus vigorously being explored beyond Si, in order to overcome performance limiting issues of Si-based transistors and CMOS technology.

Among these materials, carbon-based nanostructures are gaining increasing attention from the semiconductor industry [**1**] as viable alternatives to traditional materials used in the Si integrated-circuit (IC) industry. Such materials include the exploration of carbon nanotubes (CNTs), carbon nanofibers (CNFs), Y-junctions, graphene and graphene nanoribbons (GNRs), which either enable new device functionality or enhance the performance of established architectures in the IC industry. The exceptional physical properties of carbon-based nanostructures [**2**] has generally stirred intense interest in considering these materials for applications ranging from nanoscale transistors for nanoelectronics [**3**], [**4**], [**5**], [**6**], [**7**], [**8**], interconnects [**9**], [**10**], field-emission displays [**11**], biosensors [**12**], heat transporting assemblies [**13**], thermo-electric [**14**], photo-voltaic [**15**] and optical materials [**16**] platforms, as well as nano-electro-mechanical-systems (NEMS) [**17**], [**18**], [**19**] given their remarkable mechanical properties [**20**].

The origin of such extraordinary materials properties in carbon-based nanomaterials arises from the structural arrangement of carbon atoms in the crystalline lattice. Carbon possesses a diverse spectrum of allotropes that display a rich variety of physical properties. Even for the commonly-known three-dimensional (3D) form of carbon, namely diamond and graphite whose crystalline structures are shown in Fig. 1a and b, respectively, properties differ from the sp^3 bonded diamond, to the sp^2 bonded graphene from which graphite is derived. Shown in Fig. 1c is the two-dimensional (2D) form of carbon, a single graphene layer, which is a honeycomb arrangement of carbon atoms; when such layers are stacked vertically it forms 3D graphite. Single sheets of graphene have been a theoretical curiosity until recently, when Novoselov and co-workers synthesized these forms in 2004, through the mechanical exfoliation of 3D graphite [**21**]. The lowest dimensional form of carbon, namely zero-dimensional (0D) buckyballs or buckminsterfullerene C_{60} spheres were discovered in 1985 by Smalley and co-workers [**22**], for which they received a Nobel prize in chemistry in 1997.

When a 2D graphene sheet is rolled into a cylinder, a one-dimensional (1D) or quasi-1D form of carbon results, namely CNTs, whose crystalline structure is illustrated in Fig. 1e. This 1D form of carbon has captured the interest of scientists and engineers for nearly two decades since its discovery in 1991 [**23**]. This first form of CNTs synthesized using an arc-discharge process, was for multi-walled carbon nanotubes (MWNTs). Two years later, another form of CNTs, namely single-walled carbon nanotubes (SWNTs) [**24**], was discovered which is a single rolled-up sheet of graphene (Fig. 1e) having a typical diameter of 1 – 2 nm. MWNTs consist of concentric cylinders that have an interlayer spacing of 0.3 – 0.4 nm, and diameters that are at least an order of magnitude larger than SWNTs, between 10 – 30 nm. When a 2D graphene sheet is patterned into strips, as shown in Fig. 1f, another 1D or quasi-1D form of carbon results, namely graphene nanoribbons (GNRs) [**25**]. In this chapter, an overview of the properties, synthesis techniques, and applications of these two 1D forms of carbon, specifically CNTs and GNRs, is presented for their potential application in nanoelectronics, particularly for IC related applications. While conventional 2D planar or bulk Si forms the backbone of Si CMOS technology, its 1D form - Si nanowires (Si NWs) - are also now being explored due to the novel electronic and optical properties they posses; these forms are also discussed later in the chapter.

Section 1.0 will focus on the properties, synthesis techniques and applications of single, linear CNTs, while Section 2.0 will provide an overview of branched CNTs, which are known as Y-junctions and are enabling novel transistor functionalities. Section 3.0 will focus on 1D GNRs and then in Section 4.0, the use of CNTs as passive mechanical elements for nano-electro-mechanical-systems (NEMS) switches will be described for nanoelectronics and sensing applications. Finally, Section 5.0 will provide an overview of the synthesis of Si NWs for their potential application in nanoelectronics and nanophotonics.

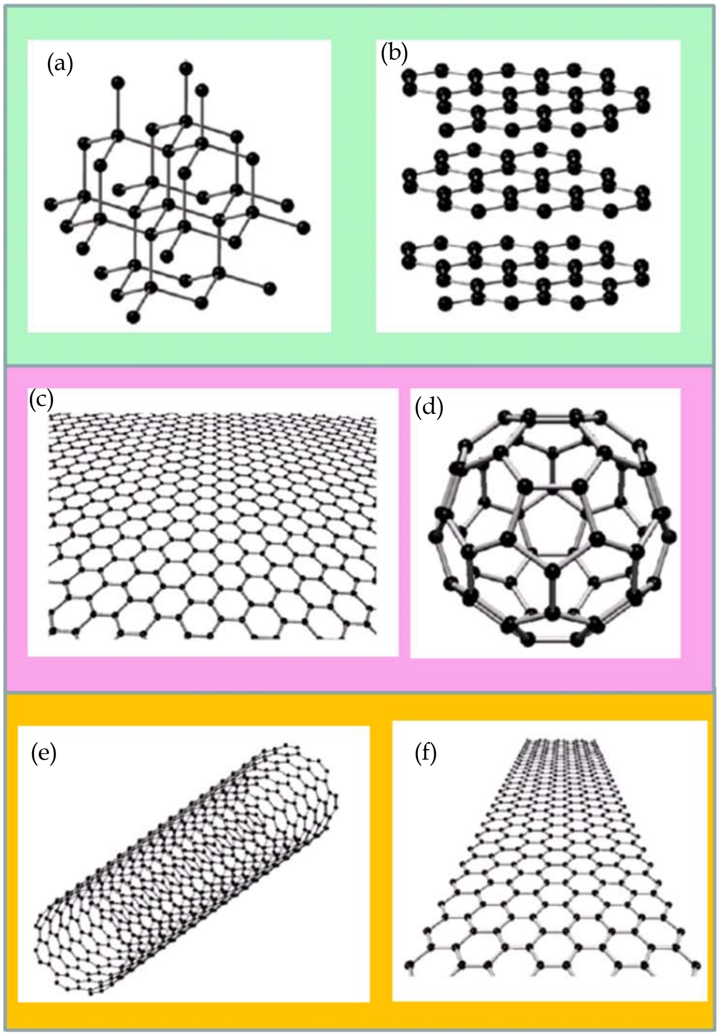

Figure 1. Crystal structures of (a) 3D diamond, (b) 3D graphite, (c) 2D graphene, (d) 0D fullerene, (e) 1D CNT (only 1-shell is shown as for a SWNT), and (f) 1D GNR. The graphene lattice in (c) is a honeycomb arrangement of carbon atoms. Depending on how this sheet is physically arranged, it serves as a building block for the other structural forms of carbon shown in (b), (d), (e) and (f). The focus of this chapter is to provide an overview of the properties, synthesis and applications of 1D forms of carbon, namely CNTs and GNRs.

The rest of Section 1.2 – 1.4 is outlined as follows. In Section 1.2, the physical properties of CNTs will be described in more detail, which is followed by the synthesis procedures of CNTs via chemical vapor deposition (CVD) in Section 1.3. Finally, in Section 1.4, the use of CNTs for transistor and interconnect applications for CMOS technology will be highlighted.

1.2 Physical Properties of Carbon Nanotubes (CNTs)

1.2.1 Electrical Properties

As mentioned previously in Section 1.1, a SWNT results when a graphene sheet is folded to form a cylinder with a seamless edge. The arrangement of the honeycomb lattice construction can differ, which determines whether the tube is semiconducting, metallic or a small-gap semiconductor. When the atoms along the circumference of the CNT are arranged in an arm-chair pattern, such nanotubes are denoted as "arm-chair" CNTs, while atoms arranged in a zig-zag fashion along the circumference are denoted as "zig-zag" CNTs; these arrangements are illustrated pictorially in Fig. 2. Tight binding approximations have been used to calculate the band structure from the specific structural arrangement of the atoms in the crystalline lattice, from which the physical properties of the tubes have been ascertained [**26**]. It was then determined that arm-chair tubes are metallic, whereas zig-zag tubes were predicted to be semiconducting. In general, when SWNTs are indexed by the number of lattice vectors n around the circumference, it was predicted that (n, n) tubes are metals, $(n, n + 3i)$ tubes (where i is an integer) are small gap semiconductors; in the latter case the energy band gap E_g scales as $E_g \sim 1/R^2$, where R is the radius of the tube, but for larger tubes the scaling can also occur according to $E_g \sim 1/R$ [**27**]. Experimentally, scanning tunneling microscopy (STM) has yielded a close agreement between the structure of SWNTs and their electronic properties [**28**], [**29**], where E_g can be as large as ~ 0.6 – 0.7 eV for SWNTs with diameters of ~ 1.4 nm [**30**].

Unique quantum phenomena have also been observed in SWNTs, such as quantum confinement and single electron charging from Coulomb blockade [**31**]. Here, the contacts to the SWNTs play an important role for displaying such quantum scale phenomena at low temperatures. The role of the electrical contacts to CNTs is discussed in more detail in Section 1.4.1, and the emergence of low temperature phenomena in CNTs has implications for their application in single electron transistors (SETs) which is discussed in more detail in Section 1.4.2.

Low metal-tube contact resistances have enabled the exploration of the intrinsic electronic properties of SWNTs, revealing ballistic transport [**32**], which was also validated by Bachtold and coworkers [**33**]. The ballistic transport is indicative of minimal electron scattering within SWNTs, which potentially arises from the reduced dimensionality for phonon scattering in 1D systems and the bonding characteristics of CNTs. This weak electron-acoustic phonon coupling in semiconducting SWNTs is also believed to be the reason for yielding the high carrier mobilities ~ 10, 000 $cm^2V^{-1}s^{-1}$ in SWNT-based field-effect-transistors (FETS) [**34**]. At higher bias voltages, the electrons have a higher likelihood of being backscattered from the high-energy optical phonons, which is also responsible for determining the maximum current carrying capability in individual metallic or semiconducting CNTs; this saturation typically occurs at ~ 25 μA [**35**] for SWNTs. The magnitude of such currents, when scaled over the cross sectional area of the tubes, gives CNTs the ability to carry the largest current densities of 10^9 A/cm^2 known of any metal, which is around 1000 times larger than that of Cu, commonly used in the IC industry for interconnect applications.

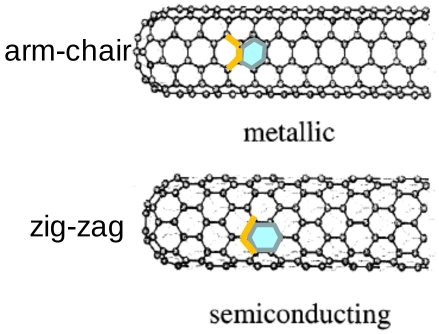

Figure 2. The electronic properties in SWNTs are strongly dependent on the circumferential boundary conditions of the hexagonal lattice which is the basis of 1D SWNTs. For example, when the carbon atoms are arranged in an arm-chair configuration (denoted schematically by the orange boundary on the lattice in the top illustration), the SWNTs are metallic, whereas when the carbon atoms are arranged in a zig-zag configuration (denoted schematically by the orange boundary on the lattice in the bottom illustration), the SWNTs have a band-gap and are therefore semiconducting.

The ballistic transport and large carrier mobilities of CNTs suggest that they are ideal candidates for field-effect-transistor (FET) applications, which is the topic of discussion in Section 1.4.3. In addition, the large current carrying capability of the nanotubes is a primary motivation for considering them as viable candidates for interconnects in the CMOS IC industry. The reduced feature sizes in CMOS ICs are forcing interconnects between each transistor to carry larger and larger current densities, which increases their likelihood of failing from electromigration. This discussion on the application of CNTs as interconnects for CMOS ICs will be discussed in Section 1.4.4.

Although not directly related to CMOS applications, in a discussion pertaining to the electrical properties of CNTs, it is also noteworthy to mention that the large current carrying capability of CNTs has created an interest in considering them in field-emission applications. In field emission, electric-field enhancement at the end of a sharp metallic tip results in the emission of electrons. Besides the higher current densities in CNT-based field emitters, the advantages that CNTs provide over benchmark Si or tungsten (W) tips, are their inherently high aspect ratio, where their strong covalent bonding which decreases their susceptibility to physical sputtering and their chemical inertness. Field emission from CNTs has potential applications as electron sources for next generation scanning-electron-microscopes (SEMs) and transmission-electron-microscopes (TEMs). In addition, the speed of an electron is 10, 000 times higher in a vacuum compared to that in the solid-state, as in a semiconductor; this has motivated the use of CNTs as field-emission cathodes in high power microwave amplifiers, such as klystrons [**36**]. The high current density of CNT field emitters has also enabled their application as electron sources for miniature x-ray sources.

1.2.2 Optical and Other Materials Properties

CNTs exhibit unique optical properties, since they possess a large, nonlinear optical absorption coefficient of light [**37**]. This arises because of their 1D band structure which gives rise to singularities in the electronic density of states. Optical absorption creates electron-hole pairs, but these rapidly fill up the low-lying bands, creating a large and nonlinear absorption coefficient. Given their typical diameters, the intrinsic band-gap in semiconducting CNTs are typically less than 1 eV which corresponds to photon energies in the infrared (IR) and makes semiconducting CNTs promising for IR emission and detection [**38**], [**39**]. In addition, arrays of vertically aligned MWNTs are promising for black-body materials [**40**] at all wavelengths. Initial optical measurements made by Yang and co-workers on the CNT arrays depicted in Fig. 3a-e, were conducted in the visible spectrum, and revealed near-perfect optical absorption, with a total hemispherical reflectance of 0.045% (λ = 633 nm) compared to 8.5% for glassy carbon which was one of the calibration standards used (Fig. 3f-h). Such measurements were extended to the longer wavelength IR region by Hata and co-workers (Fig. 3i), which revealed arrays of vertically aligned SWNTs as the "blackest" materials known, making them attractive for a variety of optical applications [**41**].

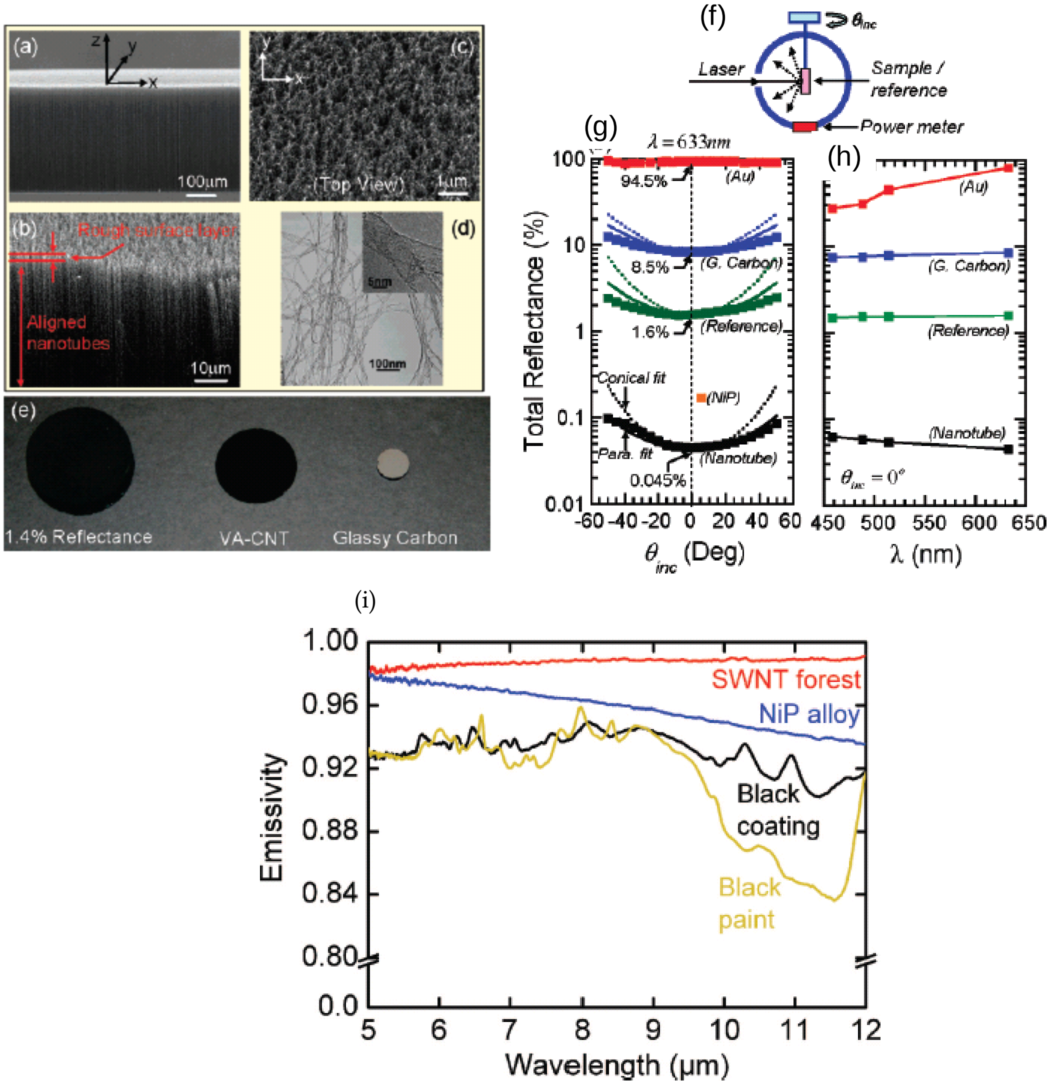

Figure 3. (a) – (c) SEM images of vertically aligned MWNTs used for the optical absorption measurements. (d) The transmission electron micrograph of the tubes yields a MWNT diameter of ~ 10 nm. (e) A comparison of the blackness for 3 samples, where the NIST standard on the left and the glassy carbon standard on the right appear less black compared to the CNT sample in the middle. (f) The measurement set-up used for the total reflectance measurements. (g) – (h) Plots of total reflectance measurements which indicates the CNT sample has a total hemispherical reflectance of ~ 0.045% at λ = 633 nm, the lowest of the other reference standards. (a) – (h) Reprinted with permission from Reference [**40**]. Copyright 2008 American Chemical Society. (i) Spectral emissivity measurements conducted on SWNT forests (red), which shows that the CNT sample is an excellent absorber even at longer IR wavelengths, when

compared to other reference standards. Reprinted with permission from Reference [**41**]. Copyright 2009 National Academy of Sciences U.S.A.

Nanotubes are also among the strongest and most mechanically resilient materials known to exist in nature. SWNTs have an extremely high directional stiffness [**42**] with a Young's modulus of ~ 1 TPa, accommodate very large mechanical strains before failure [**20**], [**43**] with a tensile strength hundred times larger than that of steel. Such exceptional mechanical properties arise from the unique sp^2 bonding in CNTs, which is similar to graphene. Calculations have revealed that the electrical conductivity of arm-chair metallic SWNTs changes only slightly for small bending angles [**44**], but at larger bending angles (~ 45^o) the electrical conductivity decreases by an order of magnitude. This has been attributed to sp^3 bonding states which arise locally in the vicinity of the bend [**45**], and lead to electron localization which reduces electrical conductance in the CNTs. In general, the exceptional mechanical properties of CNTs has created an interest for applying them in low-weight structural and conducting composites [**46**], as well as fibers [**47**], [**48**]. The large modulus and the ability of the tubes to tolerate large mechanical strains without fracture has also been a primary motivation for considering them for NEMS applications.

CNTs also possess a high thermal conductivity of ~ 6000 W/m-K [**49**], which is higher than that of other materials such as diamond which has a thermal conductivity of ~ 2000 W/m-K. The exceptional thermal properties arise in part from the conduction mechanism in CNTs which is dominated by phonons [**50**]. This is unlike conventional metals where electrons are the primary carriers of heat [**51**]. This is an important distinction, as it impacts the use of CNTs in integrated circuit applications, such as in interconnects for example, where temperatures can rise above 300 K during operation. In addition, the quantization of thermal conductance in CNTs has been observed experimentally [**52**] and agrees well with theoretical predictions [**53**].

1.3 Synthesis Techniques for Carbon Nanotubes (CNTs)

Over the years, several approaches have been implemented for synthesizing CNTs which includes arc-discharge [**24**] [**54**], laser ablation [**55**] and CVD [**56**]. Arc-discharge synthesized material generally suffers from lack of purity since it contains amorphous carbon and metal catalysts which are difficult and costly to remove. Laser methods, on the other hand, do not offer a scalable route for the large-scale production of CNTs. To date, the CVD approach has been found to result in clean, high quality tubes, and also enables a position-selective, scalable route for the on-chip synthesis of tubes, making it especially attractive for device and IC applications [**57**]. In Section 1.3.1, we provide an overview of the CVD approach for CNT synthesis, which is followed in Section 1.3.2, with a discussion on low temperature tube synthesis techniques. In Section 1.3.3, approaches used to form tubes with a high degree of alignment will then be described. Finally, in Section 1.3.4, methods used to selectively remove metallic tubes will then be discussed. All of these factors are important for enhancing the applicability of CNTs for CMOS related applications.

1.3.1 Chemical Vapor Deposition (CVD)

In CVD, a hydrocarbon gas such as ethylene (C_2H_4), acetylene (C_2H_2) or methane (CH_4) are flowed through a tube furnace over thin catalytically active transition metals such as Fe, Ni or Co. The catalytically active materials form nanoparticles at the elevated growth temperatures, in the range of 400 – 1100^{o}C [**58**]. The hydrocarbon gas molecules dissociate on the catalyst surface at high temperatures, which is subsequently followed by dissolution and diffusion of the hydrocarbon molecules into the metal nanoparticle. The carbon-saturated nanoparticle then leads to the precipitation of carbon from the nanoparticle in the form of cylindrical, sp^2 configured CNTs. An illustration of the CVD growth process is shown in Fig. 4. The specific temperature at which growth occurs is generally determined by the type of catalyst used and whether MWNTs or SWNTs are desired. The catalyst materials play an important role for the tube growth process by exhibiting a high solubility of carbon at the elevated temperatures, and typically involve metals which contain few d-wave vacancies. With this general CVD technique, tubes can grow to lengths of many millimeters (mm).

For MWNT growth, most of the CVD methods employ C_2H_4 and C_2H_2 as the carbon feedstock gas and the growth temperature is typically 550 – 750^{o}C. SWNTs generally require higher growth temperatures, and often CH_4 is used for synthesizing high quality SWNTs, since C_2H_4 or C_2H_2 decompose into a wider variety of compounds at high temperatures. Growth can also terminate from the formation of an amorphous carbon layer which coats the catalyst particle and inhibits further diffusion of carbon into the nanoparticle. To minimize this, a reducing agent such as hydrogen (H_2) or ammonia (NH_3) are also often used in conjunction with the hydrocarbon gas in order to etch or remove the excessive amorphous carbon.

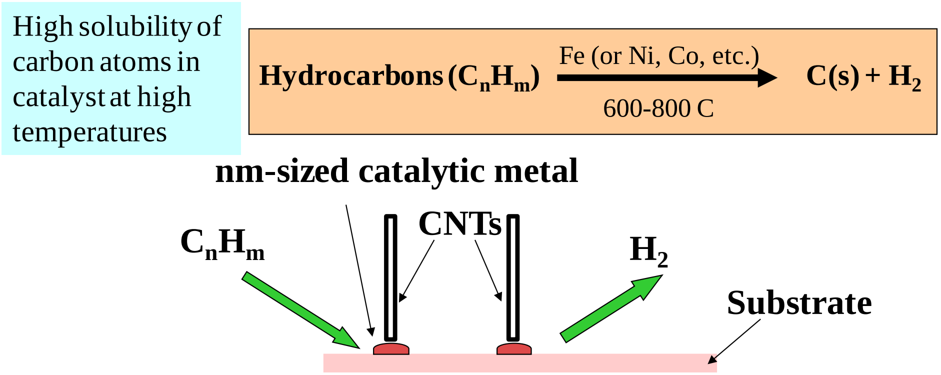

Figure 4. A schematic of the nanotube growth process using thermal CVD.

The physical characteristics of the tubes are determined, to a large extent, by the CVD growth parameters, such as the type of catalyst used and its thickness, the choice of substrate, growth temperature, pressure, as well as the type and ratio of gases used [**59**] [**60**]. All of these parameters also impact the areal density of the resulting tubes. For example, it has been found that when ethanol is used as the carbon-containing gas, the CNT density increases significantly compared to when CH_4 is used, which possibly arises from the fact that the OH radicals play a role in effectively removing the amorphous carbon from catalytic sites in the early stages of growth [**61**], [**62**].

Recently, super dense and vertically aligned SWNT forests have been synthesized over exceptionally large areas with SWNT heights of up to 2.5mm, using C_2H_2 with Argon (Ar) or Helium (He) and H_2 that contained a small and controlled amount of water vapor [**63**]. The activity and lifetime of the catalysts are dramatically enhanced by adding a small amount of water vapor in the growth atmosphere, where the water acts as a weak oxidizer that selectively removes amorphous C but does not damage the CNTs at these temperatures; an example of the resulting tubes is shown in Fig 5. With this approach, well-defined, vertically oriented structures were synthesized successfully over large length scales, as illustrated in Fig. 6, where complex 3D structures or planar 2D flexible sheets have been formed [**63**].

Figure 5. SWNT forest grown with water-assisted CVD which shows 2.5-mm tall SWNT forest on a 7 mm X 7 mm silicon chip. A matchstick is shown on the left for size reference. From Reference [**63**]. Reprinted with permission from AAAS.

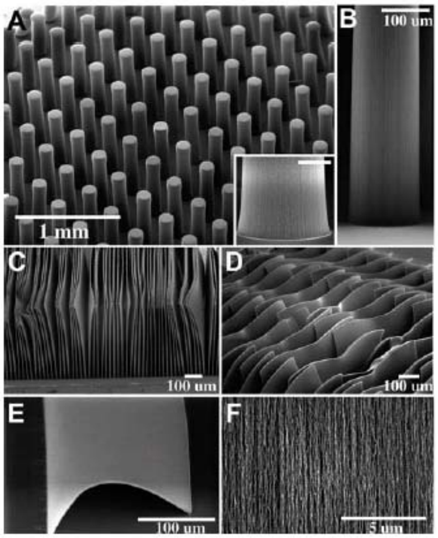

Figure 6. Water-assisted CVD has been used to synthesize organized structures as illustrated by the SEM images in (a) – (F). From Reference [**63**]. Reprinted with permission from AAAS.

1.3.2 Progress in Low Temperature Synthesis

While CNTs possess exceptional materials properties for a wide range of electronic applications, their high synthesis temperatures (generally >700^{o}C) precludes their integration with Si ICs, where temperatures have to be below 400^{o}C to make them CMOS-compatible. Several techniques have been attempted to reduce CNT growth temperatures which comprise of reactant gas modifications, appropriately engineering the catalyst, using plasmas, as well as post-growth transfer approaches.

While hydrocarbons such as CH_4 have been used to synthesize SWNTs at temperatures in excess of 850^{o}C, SWNTs have been grown at temperatures as low as 550^{o}C by using alcohols, such as methanol, instead of hydrocarbons [**62**]. In addition, pre-heating the gases to 850^{o}C facilitates gas-phase decomposition, while CNTs are subsequently synthesized at 550^{o}C on SiO_2 [**64**]. Recently, Nessim *et al.* [**65**] combined this two-phase heating approach to synthesize CNTs on conductive substrates at temperatures as low as 500^{o}C with Fe as the catalyst on a Ta under layer. In this approach, such carpets of vertically-aligned CNTs are also electrically connected to the substrate, which is important for interconnect applications; other metals such as Pd, Cu and W, also appear to be compatible.

Engineering the catalyst appropriately can also be an effective way to reduce growth temperature. For example, by using a sub nanometer thick Fe layer on SiO_2, CNT forests were synthesized at temperatures below 550^{o}C [**66**]. Binary Co/Ti catalyst have also been implemented to yield tubes at temperatures as low as 450^{o}C [**67**], [**68**], [**69**]. While Co is a commonly used catalyst for CNT synthesis, pure Co alone is not effective in synthesizing tubes at low temperatures. The melting point of pure Co is higher than that of the Co-Ti alloy, and the solubility of carbon in the binary catalyst is higher at low temperatures which yields a higher activity of carbon at low temperatures.

Elevated temperatures play a role in promoting gas decomposition, but the high temperatures also facilitate the formation of catalyst nanoparticles. The nanoparticles form as a result of thermodynamic driving forces that cause a thin catalyst film to agglomerate into nanoparticles. In the absence of such nanoparticles, CNT growth is suppressed. Recently, such nanoparticles were synthesized artificially using a custom-designed particle impactor, which is shown in Fig. 7a below. Using the impactor, Co nanoparticles 3.8 nm +/- 1.2 nm in diameter were deposited, which resulted in the formation of MWCNTs on TiN at temperatures as low as 365^{o}C. The resulting tubes are depicted in the SEM image in Fig. 7b [**70**]. While the tubes were found to nucleate at such low temperatures, they appeared to be more defective compared to those synthesized at higher temperatures. While the impactor [**70**] was important in providing a means to synthesize tubes at low temperatures, it appears that the TiN under layer also plays an important role to enhance the activities of the Co atoms in order to grow CNTs at low temperatures.

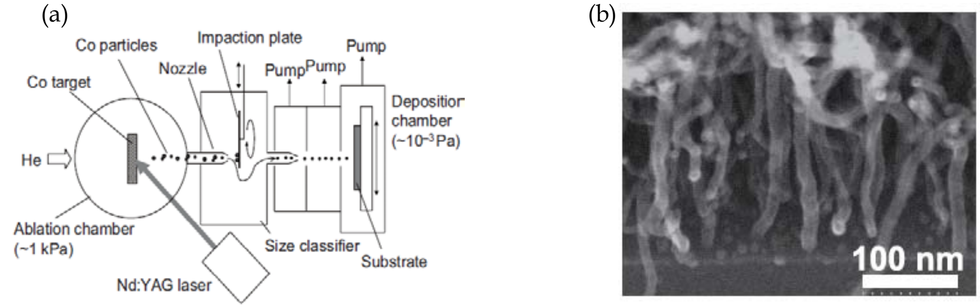

Figure 7. Low temperature synthesis of CNTs can be achieved by using a particle generation system for catalyst deposition. (a) Deposition system used for forming Co particles and (b) SEM image of MWNTs synthesized at 365$^{\text{o}}$C using the particle deposition system. Reprinted with permission from Reference [**70**]. Copyright 2009 MYU Tokyo.

Plasma based processing has also been implemented for reducing CNT growth temperature [**71**] which also provides an added benefit of improving vertical alignment within the tubes compared to thermal CVD [**72**], [**73**]; see Section 1.3.3. In general, the high energy ions in the plasma increase the likelihood of introducing defects in the tubes, although magnetic fields have been applied during synthesis to suppress this ion bombardment damage [**74**]. The growth rates in plasma processes such as plasma-enhanced (PE) CVD is also generally lower, which is likely due to the lower pressures in PECVD compared to thermal CVD. Typical PECVD growth rates are ~ 1 μm/min with saturation occurring after 10 -20 μm [**75**], [**76**], although 180 μm long CNTs were grown by dc PECVD at 700$^{\text{o}}$C using an Fe catalyst layer [**77**].

High-quality, aligned arrays of SWNTs have also been transferred post-growth onto other substrates, including low melting point, flexible, plastic sheets [**78**]. Such post-growth procedures appear to be promising as they facilitate the integration of SWNTs with a wider variety of materials that are not otherwise compatible with the high growth temperatures characteristic of conventional CVD processes.

1.3.3 Aligned Growth Techniques

For many applications, it is highly desirable to have aligned CNTs which are typically not possible to synthesize with conventional thermal CVD. However, by tuning various growth parameters within CVD, a high degree of alignment within the tubes has been observed, which makes such structures more attractive for a wider variety of applications. The approaches used for CNT alignment include the application of electrical fields during thermal CVD growth [**79**], [**80**], including those inherently present within plasmas, adjusting gas flows [**81**], [**82**], as well as using single-crystalline substrates to guide SWNT growth over nanoscale step-edges [**83**], [**84**].

With electric-field assisted growth, the CNTs align in a direction parallel to the electric field. A field strength of > 1 V/μm is typically necessary to overcome the thermally induced vibrations in growing SWNTs. Such fields can be applied externally in thermal CVD [**80**] but the field strengths are generally higher in the built-in electric-fields found in plasma processes, such as those present in the cathode dark space of a glow discharge as with PECVD. Ren and co-workers were the first to use electric-fields to synthesize carpets of vertically-oriented tubes using a plasma-based process on glass substrates [**85**]. The morphology of the structures synthesized using plasma-based processes can also result in CNFs, where the graphene layers are inclined to the central axis. Various plasma sources have been employed for tube or CNF growth, such as microwave, inductively coupled plasma (ICP), dc and dc with hot filament; a comprehensive review of the PECVD technique for tube synthesis is provided by Melechko *et al.* [**86**]. As an example, shown in Fig. 8a is an SEM image of tubes which were synthesized using C_2H_2 and NH_3 at a temperature of ~ 700°C. While unaligned and randomly oriented tubes are seen in this case, well-aligned, oriented tubes can be seen in Fig. 8b which were synthesized using dc PECVD. Similarly, in Fig. 9, a single, vertically oriented CNF is shown within high aspect ratio mesas, where the tube growth was also conducted using dc PECVD [**87**].

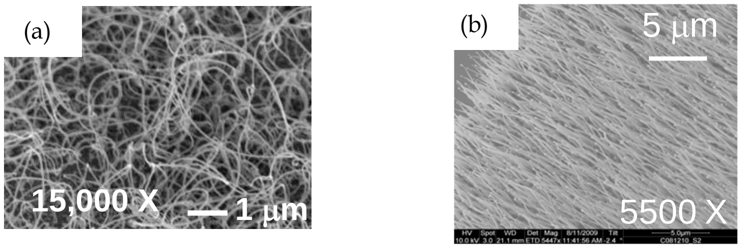

Figure 8. (a) Unaligned tubes result when C_2H_2 and NH_3 are used in the absence of an E-field. (b) An array of vertically oriented CNFs is shown for a sample that is mounted on a 45° beveled holder with respect to the electron beam in the SEM.

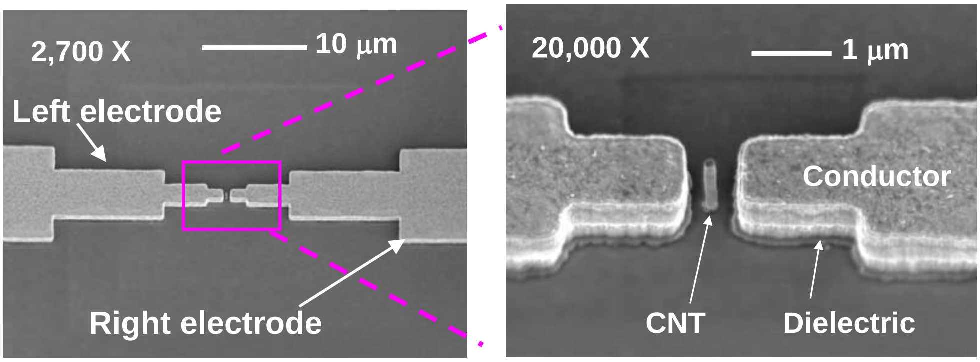

Figure 9. The low magnification image on the left shows electrodes on either side and the high magnification image on the right depicts a single, vertically aligned tube centered and < 300 nm away from the electrode. Such aligned tubes were synthesized using dc PECVD. From Reference [**87**]. Copyright 2009 IOP Publishing Limited.

The directional gas flow is another approach for aligning tubes where a thermal gradient between the substrate and the feeding gas can cause convective gas flow, which can either lift the catalyst nanoparticles or lift the SWNTs from the surface of the substrate. In this lifted configuration, the laminar flow of the incoming gases can align the air-borne SWNTs, which maintain their alignment when they land on the substrate [**81**], [**82**]. As expected, the quality of the substrate does not have a direct impact on the growth of the CNTs with this approach, and mm-long CNTs have been synthesized. However, achieving high packing density or perfectly linear shapes are issues which still need to be addressed.

Single-crystalline substrates such as c-plane sapphire or quartz can also serve as ideal templates to enable a high degree of alignment for arrays of SWNTs [**83**], [**84**]. In this approach, tubes interact with the faceted nanosteps, as small as 0.2 nm [**83**], of the single-crystalline substrate through van der Waals interactions which can guide growth along these facets. Tube lengths in excess of ~ 100 μm have been achieved, at linear densities ~ 10 CNTs/μm.

1.3.4 Techniques for Selective Removal of Metallic Tubes

The ability to preferentially form semiconducting SWNTs can be useful for many applications of SWNTs in nanoelectronics, particularly for their use in FETS. For this reason, techniques for either separating semiconducting SWNTs from metallic SWNTs, or to selectively eliminate the metallic tubes are being explored, and it appears post-growth separation techniques offer a great deal of promise [**88**].

Conventionally CVD synthesis results in an average of two-thirds (2/3) of the SWNTs to be semiconducting while the rest of the tubes are metallic. However, CVD growth parameters can be adjusted to yield a predominance of semiconducting SWNTs. For example, when ethanol/methanol were used as the carbon feedstock with Cu catalyst, 95% of the synthesized CNTs were semiconducting, which also exhibited a narrow diameter distribution [**89**]. This selective growth is thought to be due to the OH- radical from the methanol selectively etching the metallic SWNTs during growth, since the metallic SWNTs are more reactive due to their smaller ionization potential compared to semiconducting SWNTs. In addition, PECVD has resulted in the formation of 90% semiconducting tubes which were synthesized at 600ºC and yielded FETs with high ON/OFF ratios [**90**].

While growth techniques can be tailored to result in the preferential growth of semiconducting tubes, ON/OFF current ratios can also be enhanced by post-growth removal of metallic CNTs. This includes chemical removal of metallic CNTs using wet processing [**91**] or etching within the gas phase [**92**]. In the former wet-processing technique diazonium, which is an organic salt, can react preferentially with metallic SWNTs at optimized concentrations, where semiconducting SWNTs were relatively unaffected at those conditions [**91**]. However the reactivity of the semiconducting SWNTs increased at higher diazonium concentrations (> 10 μM). At optimized conditions, ON/OFF ratios ~ 10^4 were obtained with this approach, where the device mobilities did not appear to be altered when the semiconducting CNTs were exposed to the wet-process environment. Gas phase etching has also been used to preferentially remove metallic tubes with diameters between 1.3 – 1.6 at 400ºC in a CH_4 plasma [**92**]. In this process, semiconducting SWNTs with diameters > 1.4 nm are not affected, and ON/OFF ratios of 10^4 have been achieved. The metallic SWNTs are modified and broken down with thermal annealing. However, for devices that exhibit SWNTs with a wide distribution of diameters and chiralities, this technique may be restrictive due to the narrow range of diameters over which metallic SWNTs are removed, without affecting the semiconducting SWNTs.

Preferential destruction of metallic SWNTs has also been achieved with photo-oxidation using laser irradiation [**93**]. Here, when the wavelength and power-intensity of the laser are optimized, sparsely distributed metallic SWNTs are selectively removed compared to semiconducting SWNTs. More recently, it has also been shown that metallic SWNTs are destroyed faster compared to semiconducting SWNTs with the use of long-arc Xe-lamp irradiation under ambient conditions [**94**]. Recently, microwaves have also been utilized for the selective removal of metallic SWNTs [**95**]. Besides these techniques, metallic tubes can also be removed using post-growth electrical breakdown [**96**]. In this technique, the semiconducting SWNTs are reverse-biased, which causes current to be diverted through the metallic SWNTs; the large currents through the metallic SWNTs causes them to selectively burn in ambient in the presence of oxygen. This technique has resulted in ON/OFF ratios of ~ 10^5, but the Joule heat produced by adjacent metallic SWNTs appears to damage the semiconducting SWNTs as evident from their reduced carrier mobilities.

1.4 Carbon Nanotubes For Transistor and Interconnect Applications

Silicon-based FETs have been the cornerstone of the ICs industry, for applications that range from microprocessors, solid-state memories, or mobile phones. However, for the reasons already discussed, CNTs could be considered as viable materials for CMOS applications, specifically as a channel materials in FETs due to their exceptional electronic properties. In addition, CNTs are useful for interconnects due to their high current carrying capability, since Cu-based interconnects suffer from electromigration problems which are exacerbated with further scaling. In this section, the application of CNTs for transistors and interconnects will be discussed in more detail.

It is important to shed some insight into CNT-to-metal electrical contacts, which is discussed in Section 1.4.1, since this has general implications for the applicability of CNTs in FETS and nanoelectronics in general. This is followed with a discussion in Section 1.4.2 on quantum effects, such as coulomb blockade, which are observed at low temperatures and have potential applications in SETs. Then in Section 1.4.3, an overview the latest developments in CNT FETS for digital circuit applications, as well as for analog RF applications, is provided. Finally, Section 1.4.4, concludes with a discussion on the application of CNTs in interconnect technology.

1.4.1 Electrical Contacts to CNTs

The conduction properties of CNTs are intimately tied to the nature of the electrical contact between the CNT and the metal electrode, as well as intrinsic conduction within the tube body. In the absence of electron scattering and ideal electrical contacts, the conductance in SWNTs approaches the quantum limit characteristic of 1D systems, specifically $4e^2/h$ ~ 6.5 kΩ, where e is the electron charge and h is Planck's constant. Imperfect contacts give rise to an additional contact resistance R_c, and the presence of scattering centers, such as defects, within the tube body give rise to another source of resistance R_s that depends on the mean-free path and the length of the tube. The total resistance R is thus the sum of these three contributions, specifically $R = h/4e^2 + R_c + R_s$. For ideally contacted devices, when the length of the conductor is smaller than the electronic mean free path, the electronic transport is ballistic. Ohmic contacts to individual metallic SWNTs have enabled the observation of ballistic transport in SWNTs where conductance was seen to reach the quantum limit [**97**]. In such a case, Joule heat was dissipated in the electrical leads or the contacts to the tubes rather than within the CNT [**98**].

If the contacts to the tubes are non-ideal, R_c can be high and will dominate the overall contribution to the total resistance R. The measured resistance values reported in the literature range from 10^3 to 10^6 Ω at room temperature, and depends on the metals used for the electrodes. While the sp^2 bonding in CNTs gives them their exceptional electrical and mechanical properties, their closed surface makes them relatively unreactive to many materials; this makes it difficult for many materials to wet the sidewalls of the CNTs to form intimate contacts. In fact, many metals, particularly those with no d-electron vacancies, such as Al, Au, Pb have very little affinity for carbon which is evident from the fact that large discontinuities arise on the surface of SWNTs when such metals are placed on top of the SWNTs [**99**]. However, metals with many d-band vacancies, such as Ti and Nb, appear to have a greater affinity for carbon and tend to form stronger chemical bonds with CNTs.

While Ti wets SWNTs readily, in many cases annealing to high temperatures is necessary to reduce contact resistances. For example, a pronounced decrease in resistance is seen for Ti contacts to CNTs if annealed at 800°C [**100**]. The origin of the resistance decrease is presumed to be due to the formation of TiC which occurs at temperatures over 700°C, while annealing Au contacts to these temperatures has very little effect in reducing contact resistance, possibly due to the lack of chemical reactivity of Au with carbon. However, the contact resistances with Ti electrodes are not always reproducible and vary substantially from run-to-run. This may arise from the high propensity of Ti for oxidation which makes the Ti-CNT interface more susceptible to deposition conditions, such as the quality of the vacuum. More recently ohmic contact to semiconducting SWNTs has been achieved with metals such as Cr or Pd electrodes [**101**], without the need for annealing.

The typical work function φ in CNTs φ_{CNT} has been determined to be slightly below 5.0 eV [**102**]. In order to form an ohmic contact, a metal with a higher work function than the CNT is necessary (assuming p-type CNTs), such as Pd (φ_{Pd} ~ 5.1 eV), Pt (5.65 eV) and Au (5.1 eV), where the Fermi level lines up with the valence band of the CNT, forming a p-channel. Similarly, when the work function of the metal is less than the CNT, a Schottky-barrier arises for p-channel conduction. Recently, it has also been shown that Scandium (Sc) which has φ_{Sc} ~ 3.3 eV forms an n-channel in SWNTs [**6**]. Thus, by choosing the work function appropriately, Schottky diodes have been realized where a single semiconducting SWNT is contacted by a lower work function metal on one side and a higher work function metal on the other side, without the need for doping the tube [**6**].

Besides the contact resistance R_c, scattering from defects can also dominate the overall resistance contribution since R_s will be high. Recent measurements for Pd contacted CVD-grown SWNTs shows that the mean free path for defect scattering can be up to 4 μm [**103**], but mean free paths ~ 1 μm can be quite typical. Defects can also arise in the form of mechanical bends, which are especially apparent in longer SWNTs with small diameters (< 1.5 nm), and increases the potential for scattering and thus weak localization effects that suppresses conductance. In addition, contact resistance for 14 different electrode metals has been analyzed recently for a wide range of work functions from 3.9 eV to 5.7 eV, where the wettability of the metal to the CNT was also taken into consideration [**104**].

1.4.2 *Electronic Transport Mechanisms at Low Temperatures and Single Electron Charging*

At low temperatures, SWNT devices exhibit a number of interesting quantum phenomena, which are in part determined by the transparency Tr between the electrical contacts and the CNT [**105**]. For low transparency contacts ($Tr<<1$, where $G = Tr.\ 4e^2/h$) the CNT forms a quantum dot which is weakly coupled to the leads. Charge transport is then determined by the sequential tunneling of single electrons from the contacts, in the so-called Coulomb blockade regime. When Tr is increased, higher order tunneling processes, or co-tunneling becomes important which leads to the appearance of the Kondo effect. At transparencies approaching $Tr = 1$, the ballistic transport regime is encountered, where residual backscattering at the contacts leads to the observation of Fabry-Perot like resonances [**106**]. Conduction in CNTs at low temperatures can scale with temperature T in a variety of ways depending on the mechanism that governs transport. For example, for ideal contacts, a Luttinger-Liquid behavior characteristic of electrons in 1D systems follows a power law dependence where the electrical conductance G scales as $G \prec T^{\alpha}$ (α = 0.33-0.38) [**107**]. In cases where defect density may be large within the CNT, the electrons can get localized and conduction can happen through thermally activated hopping, where $LnG \prec \frac{E_a}{k_B T}$, and E_a is the activation energy for electron localization and k_B is the Boltzmann constant. When $G(T) \sim Ln\ T$, weak electron localization effects dominate electronic transport within the tubes.

Some of the quantum phenomena mentioned above has relevance to device applications. For example, the Coulomb blockade regime or single electron charging in CNTs has applications for SETs, where the motivation has been to form such transistors operational at room temperature. In the Coulomb blockage regime, transport occurs via individual electrons, where quantized energy levels exist for electrons in a

CNT, similar to those found in the "particle in a box" analogy. By applying a gate, transport between the source and drain contacts can be modulated which forms the basis for SET operation. Single electron transistors operating at room temperature have been pursued actively with Si and metal systems [**108**], [**109**]. CNTs offer another potential path for realizing high performance SETs due to their small physical dimensions which enables a large charging energy U such that $U = \frac{e^2}{2C} > k_B T$ [**110**] where C is the capacitance of the CNTs. The capacitance can be very small (aF range), which implies the energy needed for adding an electron to the system e^2/C will be large such that it exceeds the thermal energy, $k_B T$. The capacitance of a CNT scales linearly with the inverse of its length, and for a 1 μm long CNT, the single-electron charging energy is sufficiently high for coulomb blockade to be observed at liquid Helium (LHe) temperatures [**111**]. For room temperature operation, single electron charging will require a tube with length ~ 10 – 50 nm, so that U > 100 meV ~ $4k_B T$ (300K). Progress in this direction has enabled charging energies of ~ 22 meV to be achieved in SWNTs coated with silicon nitride (SiN) [**112**].

Doping SWNTs has been demonstrated to be an effective means to potentially increase charging energy. In general, doping in SWNTs can occur with electron withdrawing species such as Bromine (Br_2) and Iodine (I_2), and donating species such as Potassium (K) and Cesium (Cs) [**113**], [**114**]. In particular, semiconducting SWNTs are very sensitive to K-doping, where a transition from *p*-type to intrinsic, and intrinsic to *n*-type, is observed as the K atoms absorb onto the outer surface of the CNT and donate electrons to the tube [**115**], [**116**]. Low temperature measurements of K-doped SWNTs reveal coulomb blockade at temperatures as high as 160 K which correspond to a charging energy U ~ 50 meV. The size of the quantum dot in this case was determined to be 0.1 – 0.15 μm smaller than the physical length of the tube (~ 0.4 μm). This phenomenon was attributed to the inhomogeneous K-doping profile along the CNT. To form high temperature CNT-based SETs a reliable approach needs to be developed to uniformly yield tube lengths in the tens of nm range, and suggests that with continued development, room temperature SETs may be a possibility in the near future.

1.4.3 Carbon Nanotube Field-Effect-Transistors for Digital and Analog Applications

As the channel length of the transistor is reduced to the current scale of ~ 35 nm, the thickness of the gate dielectric also needs to be reduced. This is necessary to ensure that the carrier density in the channel is controlled by the transverse electric field from the gate rather than by the lateral source-drain electric field. As the gate dielectric thickness is reduced to below 2 nm however, charge leakage due to quantum mechanical tunneling increases, which causes higher leakage currents; the power consumption and heat dissipation are also concomitantly high. If the thermally grown SiO_2 layer that is normally used for the gate dielectric is replaced with a deposited metal oxide with larger permittivity, such as HfO_2, the leakage currents can be reduced. This is possible since a thicker dielectric layer can be used to yield the same gate capacitance. However, the interface quality with deposited barriers is generally poorer compared to thermally grown barriers such as SiO_2, which causes the carrier mobilities in deposited barriers to be reduced [**117**]. It should be evident from this discussion, that alternative semiconductors are necessary, which exhibit higher carrier mobilities and increase performance while being compatible with Si IC technology at the same time. For this reason, the large carrier mobilities inherent in carbon-based nanomaterials such as SWNTs and more recently GNRs, has been the main driving force for considering them for FET applications.

The first CNT-FETS were demonstrated in 1998, which showed transistor behavior at room temperature, where conductance changed by six orders of magnitude when a gate voltage was applied [**118**]. A schematic of this first FET transistor is shown in Fig. 10a where the SWNTs were dispersed onto an oxidized Si wafer onto lithographically defined Pt electrodes. The SWNTs served as the "channel" region indicated by (B), and the Pt electrodes were the equivalent to the source and drain, which is represented by the regions marked (A) and (C), respectively, in Fig. 10a. The electrical response of this transistor is shown in Fig. 10b, which indicates a conductance change > 10^6 as the gate voltage was varied. In these first FETs, the Si substrate was used as the bottom gate electrode and was common to all the FETS on the wafer and the SiO_2 gate oxide was very thick (~ 100 – 150 nm). Due to the difficulty of forming more complex integrated circuits with this architecture, the next generation FETs had independent top-gates on each SWNT [**119**]. The performance characteristics of the top-gated FETS were found to be better, as they exhibited a lower threshold voltage $V_t \sim 0.5$ V, compared to a $V_t \sim -12$ V for the bottom-gated devices, in addition to a higher drive current. After comparing the performance metrics to conventional Si devices when normalized for the channel width, these CNT-FETs had a resulting figure of merit which was 20 times larger than the existing CMOS devices [**119**].

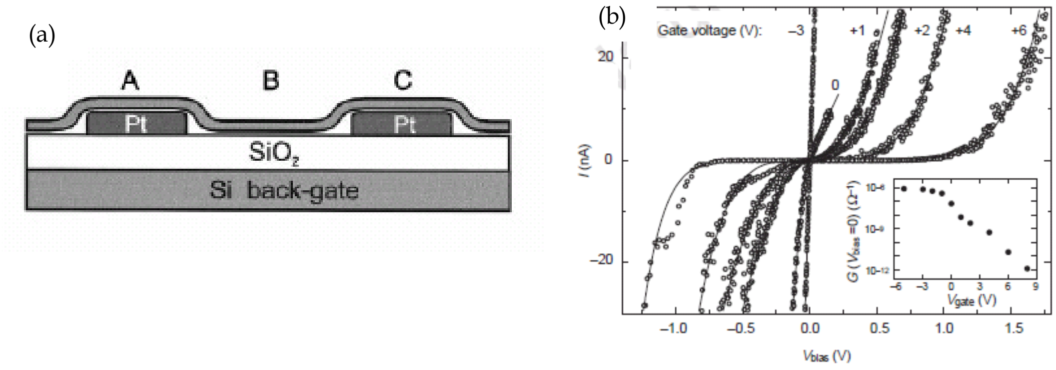

Figure 10: (a) A schematic of the first CNT FET where a semiconducting tube serves as the channel in region (B) and is contacted by Pt electrodes which serve as the source and drain (denoted by regions A and B). (b) The gating response of the CNT FET. Two terminal measurements of the source-drain current at various gate voltages. Inset shows conductance at $V_{bias} = 0$ V as a function of V_{gate}, where the conductance varied over six orders of magnitude. Reprinted by permission from Macmillan Publishers Ltd: Nature, Reference [**118**], copyright 1998.

As with conventional FETs performance is improved by increasing the capacitive coupling of the gate electrode by either reducing the thickness of the gate dielectric or using a dielectric with a higher permittivity compared to SiO_2. Excellent transistor performance metrics have been achieved with the use of high-κ dielectrics such as ZrO_2 for the gate oxide deposited using ALD [**120**], [**121**], TiO_2 [**122**] or HfO_2 [**123**]. The corresponding SWNT-FETs display a sub-threshold swing close to the theoretically expected value of S = 60 mV/decade (at 25^oC), along with a large transconductance of ~ 5000 Sm^{-1}. In addition, the use of organic self-assembled monolayer (SAM) coatings has also yielded SWNT-FETs with exceptional performance [**124**].

It is generally believed the SWNT FETs do not behave as bulk transistors, but are more akin to Schottky-barrier transistors. In the latter, the applied gate voltage modulates both the carrier density and the transmission through the Schottky barriers at the contacts which affects the channel resistance [**125**]. However, Schottky barriers at both of the CNT–metal junctions are difficult to remove and severely limits the 'ON' state conductance and also reduces the current delivery capability, compromising the overall transistor performance. As discussed in Section 1.4.1, the use of Pd has been shown to greatly reduce this Schottky barrier due to its high work function relative to the CNT, and also its ability to wet the tubes readily [**101**].

Progress has also been achieved in the circuit-level applications of SWNT-based FETS. A CMOS-like voltage inverter or logic NOT gate was demonstrated with an inverter circuit comprising of *n*- and *p*-CNT FETs [**126**]. The significance of this accomplishment relies on the fact that CNTs are inherently p-type from oxygen doping, and for CMOS-applications, both *n*- and *p*-type FETs are desirable. In early work done in forming *n*-type FETs, one of the tubes was covered with a protective film of PMMA, while the other tube was unprotected and annealing in vacuum transformed both of the CNT FETS to *n*-type. Upon cooling, and subsequent exposure to oxygen, the unprotected CNT-FET was converted to *p*-type, while the protected one remained *n*-type. In this way, two complementary CNT-FETs were formed and an inverter circuit was demonstrated; this was referred to as an intermolecular inverter because two CNTs were involved. Circuits have also been formed along the length of a single CNT, which results in potentially higher integration densities. Such circuits are referred to as intramolecular circuits since two complementary FETs are formed along the same tube. This was achieved by opening a small unprotected portion of the tube that was doped with potassium to transform it into *n*-type [**127**]. Using this technique, an inverter circuit was fabricated on the same tube which exhibited a gain of ~ 2 for relatively unoptimized tubes and more complex circuits have been formed along the length of a single CNT [**128**]. Recently, contact to the SWNT's conduction band has been accomplished using Sc with its very low work function, which enables the formation of both *p*- and *n*-type SWNT-FETs, and should provide an elegant means for realizing circuit-level applications [**6**].

In the transistor applications of CNTs described above, a semiconducting tube is desired but it is difficult to obtain 100% semiconducting tubes using conventional CVD approaches, although some progress has been made in this regard, as described in Section 1.3.4. Recently, using post-growth transfer techniques, ordered arrays of CVD grown tubes were placed onto polymer substrates and electrical breakdown was used to remove the metallic tubes [**129**]. The transistor devices on the transferred substrate displayed good performance with carrier mobilities ~ 1000 $cm^2V^{-1}s^{-1}$, scaled transconductances as high as 3000 Sm^{-1} and current outputs of 1 A. A polymer-based amino group was used to form *n*-type FETs, and by combining the *p*- and *n*-type FETs, various CMOS-based logic gates have also been realized. Integrated circuits based on SWNT-FETs have also been fabricated on flexible plastic substrates, which marks a major milestone for the larger-scale integration of SWNTs for nanoelectronics applications [**130**].

The applications described above are primarily for digital circuits which has been the main focal point for the end-use applications of CNT to potentially replace Si-CMOS technology. However, presently the growth and fabrication technology for CNT-FETs is still not sufficiently mature enough, particularly for *as-grown* tubes, to justify their insertion in very-large-scale-integration (VLSI) technology which has more stringent tolerance requirements. However, due to the more relaxed manufacturing tolerances and less stringent device performance metrics required for RF analog systems, such as wireless communications, these applications may be better suited for a more near-term insertion of CNTs for realizing commercial systems. In particular, CNT-FETs are predicted to have an inherent linearity as reported in [**131**], which is a critical metric for determining the suitability of SWNT-FETs for wireless communication applications.

For RF-FET applications, massively-parallel, aligned arrays of CNTs are necessary to improve impedance matching, increase the transconductance, the ON-state current, and the power density of the devices; a schematic of such a FET is shown in Fig. 11a [**132**]. For arrays of CNTs, the effective mobility is determined by the CNT density, alignment, and the fraction of semiconducting SWNTs, and the parasitic capacitances have been taken into consideration in developing a small-signal model of such a structure for RF applications [**132**]. The high-frequency performance of CNT FETs has progressively improved, with individual CNT FETs reaching frequencies up to 52 MHz in a multistage ring-oscillator [**133**] and arrays of CNTs showing cut-off frequencies larger than 10 GHz [**129**], [**134**], [**135**], [**136**], [**137**]. The highest frequencies reported so far have been for samples comprising of tube arrays with mixed semiconducting and metallic tubes grown with CVD on quartz [**135**], [**138**], as well as for samples that with 90 -95% metallic tubes with higher areal densities which were deposited using dielectrophoresis [**136**].

Recently, progress has also been made in the application of such devices in RF radio systems, for example, where a nanotube was used as the demodulator in a radio receiver [**139**]. A schematic of the measurement set-up is shown in Fig. 11b, where the nanotube detected an amplitude-modulated (AM) signal, and replaced the diode in a classical AM radio. In related work on CNT radios, the mechanical resonance frequency of the CNT was used as an integrated RF filter, although the measurement was conducted in a high vacuum environment in this case [**140**]. Recently, an RF amplifier based on a CNT FET was also built where an entire AM radio system was demonstrated [**138**], marking a major milestone in the application of CNTs into fully functional RF systems.

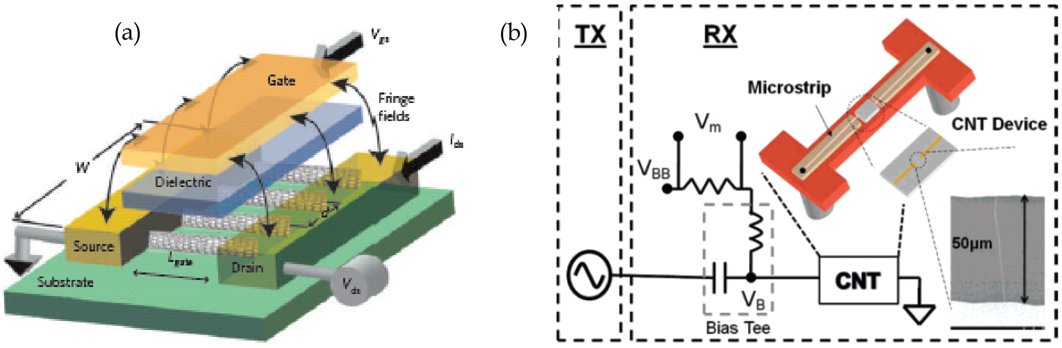

Figure 11. **(a)** Schematic showing an array of SWNTs which serve as the channel region in a CNT FET. For RF applications, aligned arrays of CNTs yield superior impedance matching characteristics compared to single tube devices which exhibit high contact resistances. The array of tubes also increase the transconductance, the ON-state current and the power density of the device. Reprinted by permission from Macmillan Publishers Ltd: Nature Nanotechnology, Reference [**132**], copyright 2009. (b) Schematic of the test-setup for the CNT-based AM demodulator. Inset shows the SEM image of the CNT on the right. Reprinted with permission from Reference [**139**]. Copyright 2007 The American Chemical Society.

1.4.4 Carbon Nanotube Interconnect Technology

With continued feature size reduction in Si ICs, interconnects based on the Cu dual damascene technology are encountering fundamental challenges as a result of the exceptionally large current densities that are forced through them. The large current density makes the Cu interconnects prone to failure by electromigration. Additionally, Cu is susceptible to diffusion into the surrounding dielectric, which reduces the effective cross sectional area for electrical conduction, and complicates processing since a spacer or barrier layer is necessary to minimize such diffusion. The small cross sectional areas of the interconnects causes the resistance to also increase, which induces larger delays to signal propagation through an effective increase in the resistance-capacitance (RC) time constants. At the 130 nm technology node, more than 70% of capacitance on a high-performance chip is associated with interconnects, making the dynamic power dissipation from interconnects larger than that of the transistors [**141**]. Scaling of dimensions in ICs in order to enable gigascale integration thus poses an undue burden on interconnects based on the Cu dual damascene technology, and new materials, such as CNTs, are being explored to overcome such challenges.

As cross sectional dimensions in Cu interconnects approach the mean-free-path for electron scattering, metal resistivity increases and surface scattering plays a dominant role [**142**]. The degree of scattering in this regime depends on the quality of the surface, and can cause electrons to lose longitudinal momentum as they get scattered by the wire surfaces. On the other hand, multi-channel ballistic conduction has been observed in MWNTs over distances of several μms in contrast to Cu which has a mean free path of ~ 40 nm at 25°C [**103**]. The reduced dimensionality for phonon scattering in 1D quantum wires such as CNTs [**143**], minimizes small-angle scattering unlike in conventional wires where electrons can experience small angle scatterings and thereby dissipate energy. As already mentioned, CNTs also possess a high current carrying capability ~ 10^9 A/cm^2, more than 1000X larger than that of Cu, which makes them less susceptible to failure by electromigration. Their higher chemical stability relative to Cu mitigates the need for a diffusion-barrier via spacer layers. The large mean free path, high current carrying capability, resistance to electromigration and the general chemical inertness of CNTs, makes them an attractive candidate material for interconnect applications for the gigascale era [**144**], [**145**].

In order to reduce the overall resistance, multiple CNTs in parallel are required, which also has the potential to minimize the effects of any Schottky barrier that may exist between the bundles and the electrical contacts. For the rest of this section, we describe recent progress made in the modeling of CNTs for interconnect applications, where the quantum-scale properties of the CNTs are also taken into consideration. We close this section with a report on the synthesis of CNT bundle interconnects, where consideration is given to low synthesis temperatures and growth on conducting substrates.

In a conventional current-carrying wire, the total energy is a sum of the energy stored in the magnetic field which is signified by the magnetic inductance, as well as the kinetic energy (KE) of the moving electrons themselves which leads to an inductive term denoted by the so-called kinetic inductance. In conventional wires, the latter is much smaller than the former and the kinetic inductance is thus ignored. However, in CNTs the KE of electrons can be substantially larger than the energy stored in the magnetic field, causing the kinetic inductance to be much larger; for example, the kinetic inductance in a SWNT can be more than 4 orders of magnitude larger than the magnetic inductance. The kinetic inductance of the electrons per unit length of a quantum wire l_K has been calculated to be $l_K = h/4v_F e^2$, where v_F = 8 x 10^5 ms^{-1} (for graphene and hence CNTs) and l_K for SWNTs ~ 4 nH/μm [**146**]. High-frequency measurements have confirmed the existence of the kinetic inductance, and the measured values are close to those obtained from theory [**147**].

While SWNTs exhibit large inductances which can be useful for on-chip inductors, their benefits as interconnects are especially apparent at high frequencies. At high frequency the resistance of a metal wire increases significantly due to skin effect losses. High frequency analysis of CNT interconnects reveals that due to the presence of a large kinetic inductance, the skin effect is reduced which makes it a very promising interconnect material for future high-frequency IC applications [**148**]. The quantum and electrostatic capacitances C_Q and C_E, respectively, have also been calculated in CNTs where C_Q ~ 200 aF/μm per conduction channel, and in virtually all cases $C_Q > C_E$. Following this analysis, a circuit model of CNTs has been developed (Fig. 12) where the quantum-scale parameters of the tubes have been taken into account [**144**]. This analysis has been implemented to collectively evaluate the performance of SWNT and MWNT bundle interconnects, where the overall conductivity has been determined as a function of the physical dimensions of the tubes. The modeling and application of MWNTs and SWNTs interconnects has been discussed in detail by Naeemi *et al.*, [**141**], [**149**] and the performance has been benchmarked relative to Cu interconnects.

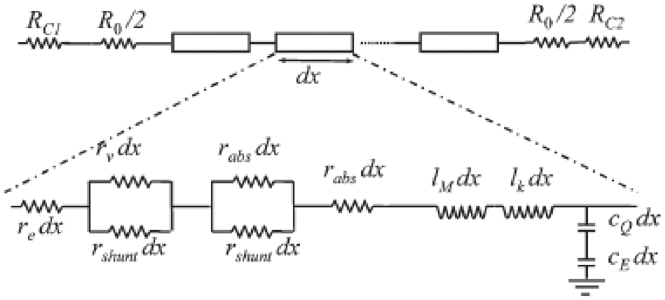

Figure 12. An equivalent circuit for a nanotube where the tube parameters such as the electrostatic capacitance, quantum capacitance, kinetic inductance and magnetic inductance, which have been taken into consideration and are used for modeling the performance of CNTs for interconnect applications. Reproduced with permission from Reference [**144**]. Copyright 2008 IEEE.

Experimental reports on CNT-based interconnects consist of utilizing a bottom-up approach to synthesizing vertically-oriented tubes using CVD, where etch-back of the SiO_2 layer was used with CMP to form vertical interconnect vias [**9**]. In prior work, CNT growth in high-aspect ratio vias was also demonstrated [**150**]. From a practical standpoint, multiple CNTs in parallel on conductive substrates are required to lower the overall resistance compared to an individual tubes. In this case, for CNT interconnects to outperform Cu, SWNT/MWNT densities of at least ~ 3 x 10^{13} CNTs/cm^2 are desired. One of the challenges for interconnect applications is that the maximum packing densities in CNT bundles is still ~ 2 orders of magnitude lower than desired. Since MWNTs exhibit multiple channels of conduction, the packing density required may be lower with MWNTs compared to SWNTs; however contact to all the shells within MWNTs is desired.

Issues with CNT-based interconnects which are currently under exploration, include enhancing catalyst activity [**151**] and using the zipping effect of liquids [**152**] to increase CNT density, controlling CNT chirality [**153**], performing growth on conducting substrates at reduced growth temperatures [**154**], [**155**], [**156**] to make CNT-interconnects CMOS-compatible, as well as controlling CNT alignment with the gas-flow [**157**], [**158**]. As an example, well-aligned CNT bundles have been grown up to lengths exceeding 100 μm [**159**], [**160**] which also have applications as through-wafer vias in 3D ICs; an image of such bundles in through-wafer vias is shown in Fig. 13.

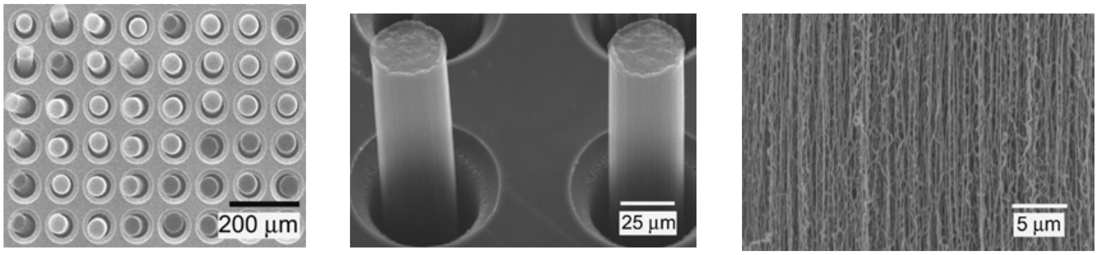

Figure 13. SEM micrographs of bundles of MWNTs under development for through wafer vias or 3D interconnects. that emerge from vias under development for 3D interconnects or through-wafer vias (viewing angle of 45°). Shown at the right is a higher magnification SEM image which depicts tube arrays within a single bundle. Reprinted with permission from Reference [**160**]. Copyright 2007, American Institute of Physics.

2.0 Novel 1D Architectures for Electronics: Y-junctions

2.1 Introduction

In recent years, carbon nanotubes (CNT) have emerged as one of the foremost manifestations of nanotechnology and extensive research has been expended in probing their various properties. While many desirable attributes in terms of electrical, mechanical, and biological properties have been attributed to CNTs, many obstacles remain before their widespread, practical, application [**161**] becomes feasible. Some of the foremost hindrances are (i) variation of properties from one nanotube to another, partly due to unpredictability in synthesis and the random occurrence of defects, (ii) lack of a tangible method for wide-scale synthesis. Generally, (i) is a natural consequence of nanoscale structures and could be difficult to solve, at least in the short term. It seems that fundamentally new ideas might be needed. Some interesting viewpoints are being considered, where defect manipulation could be used on purpose [**162**], [**163**]. Wide scale synthesis methods, for example, by aligning the nanotubes with the underlying crystal orientation [**129**] have recently proved successful, but it is still not clear as to whether such methods would allow for practical implementation, say at the scale of Silicon microelectronics.

In this context, it would be pertinent to take a pause and consider the rationale for the use of nanotubes, especially in the context of electronic characteristics and devices. Carbon based nano-electronics technology [**164**] promises greater flexibility compared to conventional silicon electronics, one example being the extraordinarily large variety of carbon based organic structures. It would then be interesting to look into the possible implications of this “large variety”, particularly with respect to morphology and associated properties. Such an outlook gives rise to the possibility of examining nonlinear forms, some examples of which are depicted in Figure 14.

While Y-junctions can be used as three-terminal switching devices or diodes, helical nanostructures can give rise to nanoscale inductors or more interestingly, a sequence of metallic and semiconducting junctions [**165**]. It is to be noted, at the outset, that we seek in our research to explore completely novel forms of electronics, as laid out for example in the ITRS (International Technology Roadmap for Semiconductors) recommendations on Emerging Research Devices. We quote *"The dimensional scaling of CMOS devices and process technology, as it is known today, will become much more difficult as the industry approaches 16 nm (6 nm physical channel length) around the year 2019 and will eventually approach an asymptotic end. Beyond this period of traditional CMOS scaling, it may be possible to continue functional scaling by integrating alternative electronic devices onto a silicon platform. These alternative electronic devices include 1D structures such as **CNTs** …"* It is the purpose of investigating novel nanotube morphologies, then to demonstrate many of the "*compelling attributes*" as laid out in the ITRS roadmap, which include (i) *"Room temperature operation"*, (ii) *"Functionally scalable by orders of magnitude" and* (iii) *"Energy dissipation per functional operation substantially less than CMOS"*. We will show specifically, how the exploration of Y-junction topologies would help in laying the foundation for an entirely new class of electronic and optical devices.

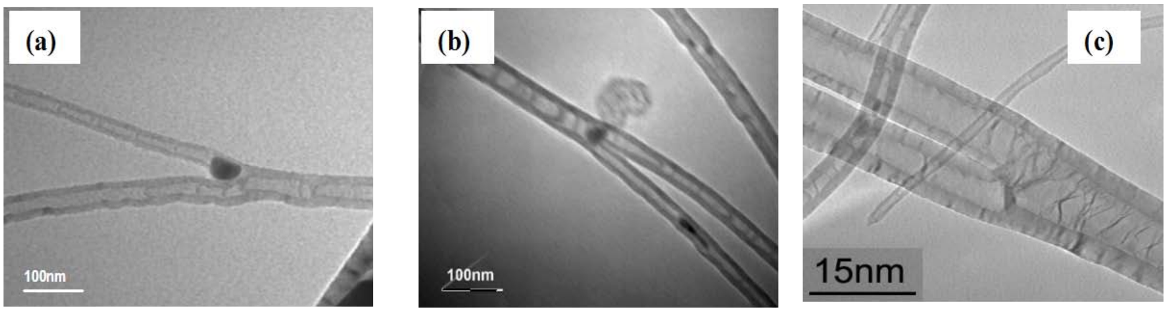

Figure 14. The ***nano-engineering*** of carbon nanotubes (CNTs) to produce nonlinear structures is manifested most clearly through the Y-junction morphology. Such structures can be prepared by adding carbide forming elements, such as Ti, Zr, and Hf to ferrocene based thermal CVD, at different branching angles (*i.e.,* a *vs.* b) and spatial locations of catalyst particles (*i.e.,* a *vs.* c) through varying the growth conditions.

2.1.1 Conventional Carbon Nanotubes

We commence with an overview of the underlying constituents of Y-shaped structures- linear nanotubes. Several comprehensive expositions of the fundamental aspects are extant in literature [**166**], [**167**], [**168**], [**169**], [**143**]. Nanotubes are essentially graphene sheets rolled up into varying diameters [**170**] and are attractive from both a scientific and a technological perspective, as they are extremely robust (Young modulus approaching 1 TPa) and, at least in pristine forms, chemically inert. By varying the nature of wrapping of a planar graphene sheet and consequently their diameter, nanotubes can be constructed to be either semiconductors or metals [**171**] which can be used in electronics [**172**]. In the literature, there are a variety of tubular structures composed of carbon, and are referred to as nanotubes (Single walled/Multi-Walled nanotubes: SWNT/MWNT) when the graphene walls are parallel to the axis of the tube, and as nanofibers for other configurations, *e.g.,* where the graphene sheets are at an angle to the tube axis.

The electrical and thermal conductivity [**173**] properties of both SWNTs [**106**] and MWNTs have been well explored. While SWNTs (diameter ~ 1 nm) can be described as quantum wires due to the ballistic nature of electron transport [**174**], the transport in MWNTs (diameter in the range 10-100 nm) is found to be diffusive/quasi-ballistic [**175**], [**176**]. Quantum dots can be formed in both SWNTs [**111**] and MWNTs [**175**] and the Coulomb blockade and the quantization of the electron states can be used to fabricate single-electron transistors [**118**]. Several electronic components, based on CNTs, such as SETs [**118**], [**177**], [**178**], non-volatile Random Access Memory (RAM) [**17**], [**179**], and FETs and logic circuits [**180**], [**101**], [**5**], have also been fabricated. However, most of these devices use conventional lithography schemes and electronics principles, either using nanotubes as conducting wires or modifying them along their length, say through Atomic Force Microscopy (AFM) based techniques [**177**]. While extremely important in elucidating fundamental properties, the above experiments have used external electrodes, made through conventional lithographic processes to contact the nanotubes and do not represent truly nanoelectronic circuits. Additionally, the well known MOSFET (Metal Oxide Semiconductor Field Effect Transistor) architecture is used, where the nanotube serves as the channel between the electrodes (Source and Drain), and a SiO_2/Si based gate modulates the channel conductance. In other demonstrations, cumbersome AFM [**177**] may be needed.

It would, therefore, be more attractive to propose new nanoelectronic elements, in order to harness new functionalities, peculiar to novel CNT forms such as nanotubes with bends, Y-junctions [**8**] etc. One can also envision a more ambitious scheme and circuit topology - where both interconnect and circuit elements are all based on nanotubes, realizing true nanoelectronics (Figure 15).

For example, nanotube based interconnect does not suffer from the problems of electro-migration that plague copper based lines, due to the strong carbon-carbon bonds, and can support higher current densities [**181**] (~ 10 μA/nm^2 or 10^9 A/cm^2 *vs.* 10 nA/nm^2 or 10^6 A/cm^2 for noble metals such as Ag). Additionally, the predicted large thermal conductivity [**182**] (~ 3000 W/mK at 300 K), up to an order of magnitude higher than copper, could help alleviate the problem of heat dissipation in ever shrinking devices. Developing nanotube based devices, besides miniaturization and lower power consumption, could also allow us to exploit the advantages of inherently quantum mechanical systems, for practical devices, such as ballistic transport and low switching voltages [**183**] (~ 26 mV at room temperature ≡ k_BT/e).

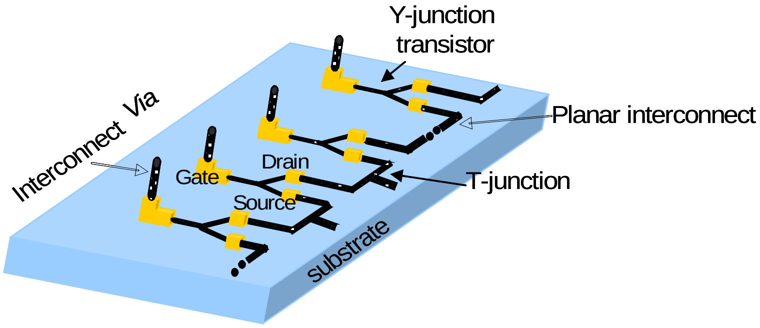

Figure 15. A conceptual view of a possible CNT technology platform, including Y-junction devices, interconnect *vias* and directed nanotube growth. The overall objective is to create nano devices with novel functionalities that go beyond existing technologies.

2.1.2 *Branched Carbon Nanostructures*

At the very outset, any deviation from linearity, say in a branched Y-junction, must be accompanied by the disruption of the regular hexagonal motif. This can be accomplished, in the simplest case, by the introduction of pentagons and heptagons to account for the curvature [**184**] (Figure 16a). Since the charge distribution is likely to be non-uniform in these regions, the interesting possibility of localized scattering centers can be introduced. For example, rectification behavior was posited due to different work functions of contacts with respect to Metal (M) and Semiconductor (S) nanotubes (electrostatic doping) on either side of the bend[13]. We will see later that how this can be exploited for more interesting device electronics.

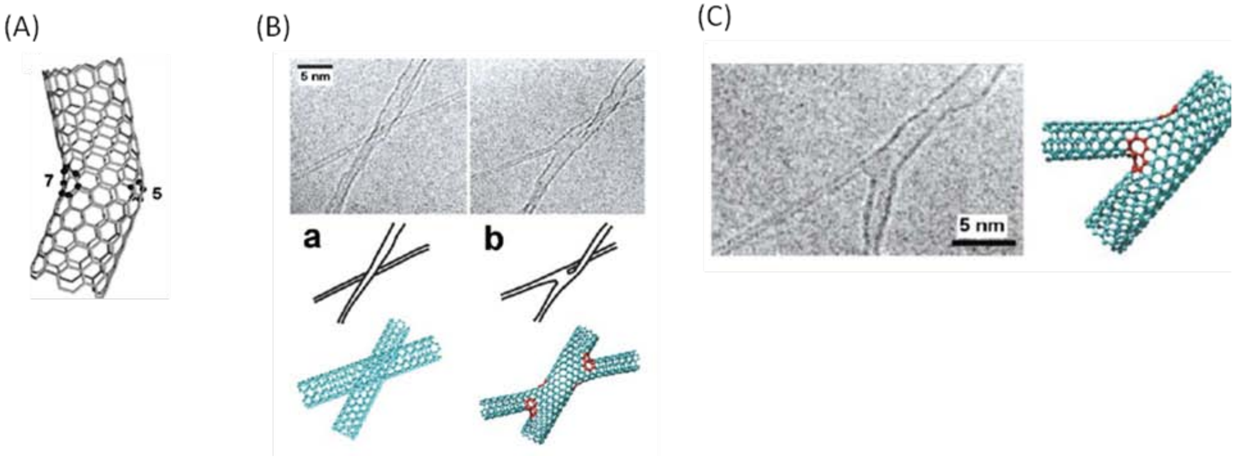

Figure 16. **(a)** A bend in a nanotube, say in a Y-junction, introduces regions of positive and negative curvature. The associated heptagons and pentagons can have local excess/deficit of charge and can be used as scattering centers for nanoelectronics. Reprinted with permission from Reference [**171**], Z. Yao *et al. Nature*, 402, 273 (1999). Copyright @ Nature Magazine, Macmillan Publishers. **(b)** X-shaped and **(c)** Y-shaped nanotube molecular junctions can be fabricated by irradiating crossed single walled nanotube junctions with high energy (~ 1.25 MeV) and beam intensity 10 A/cm^2) electron beams. Reprinted with permission from Reference [**185**], M. Terrones *et al. Phys. Rev. Lett.*, 89, 075505 (2002). Copyright @ The American Physical Society.

Nanotube junctions can be formed through the use of high energy (1.25 MeV) electron beam exposure (in a Transmission Electron Microscope) based welding of linear SWNTs, at high temperature (800 ^{o}C) welds SWNTs to form X-, Y-, or T- junctions was illustrated [**185**] (Figures 16b and 16c) The underlying mechanism invoked was primarily the "knock-off" of carbon atoms and *in situ* annealing. Molecular dynamics simulations intimate that vacancies and interstitials play a role. However, the purposeful synthesis of branched morphologies can be accomplished through CVD methods. Preliminary work on individual Y-junctions, grown through CVD, in branched nano-channel alumina templates [**186**] resulted in the observation of non-linear I-V characteristics at room temperature through Ohmic contact [**187**] and tunneling conductance [**188**] measurements. From an innate synthesis point of view, nanotubes with T-,Y-, L- and more complex junctions (resembling those in Figure 1), were initially observed in arc-discharge produced nanotubes [**189**]. Beginning in 2000, there was a spate of publications reporting on the synthesis of Y-junctions through nickelocene and thiophene based CVD [**187**], [**188**]. Y-junction [**186**] and multi-junction carbon nanotube networks [**190**] were also synthesized through the pyrolysis of methane over Co catalysts and through growth on roughened Si substrates. However, the mechanism of growth was not probed into adequately.

2.2 Controlled Carbon Nanotube Y-junction Synthesis

It is to be noted at the very outset that the Y-junctions synthesized are quite different in form and structure compared to crossed nanotube junctions [**185**], [**191**], where the nanotubes are individually placed and junctions produced through electron irradiation [**185**]. Significant control in the growth of Y-junction nanotubes [**192**] on bare quartz or SiO_2/Si substrates through thermal CVD was accomplished through the addition of Ti containing precursor gases to the usual nanotube growth mixture. In one instance, a mixture of ferrocene ($C_{10}H_{10}Fe$), xylene ($C_{10}H_{10}$) and a Ti containing precursor gas-$C_{10}H_{10}N_4Ti$ was decomposed at 750 ^{o}C in the presence of flowing argon (~ 600 sccm) and hydrogen (75 sccm) carrier gases. The two stage CVD reactor consisted of: (1) a low temperature (~ 200 ^{o}C) preheating chamber for the liquid mixture vaporization followed by (2) a high temperature (~ 750 ^{o}C) main reactor. A yield of 90% MWNT Y-junction nanotubes, which grow spontaneously on quartz substrates in the main reactor, was obtained. The mechanism for the Y-junction growth was hypothesized to depend on the carbide forming ability of Ti as measured by its large heat of formation (ΔH_f of -22 Kcal/g-atom).

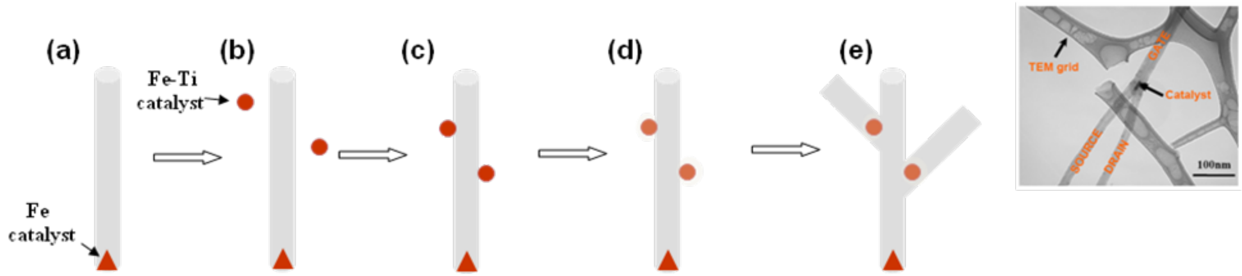

Figure 17. The postulated growth sequence of a Y-junction nanotube[41] involves: (a)Initial seeding of a straight nanotube through conventional catalytic synthesis [**193**]. (b) Ti-doped Fe catalyst particles (from ferrocene and $C_{10}H_{10}N_4Ti$) attach (c) to the sidewalls and nucleate (d) the side branches (e).

The Ti containing Fe catalyst particles seed nanotube nucleation and grow by a *root growth* method, in which carbon was absorbed at the root and then ejected to form vertically aligned MWNTs (Figure 17a). As the supply of Ti-containing Fe catalyst particles continues (Figure 17b), some of the particles (Fe-Ti) attach onto the sidewalls of the growing nanotubes (Figure 17c). The catalysts on the side then promote the growth of a side branch (Figure 17d), which when further enhanced forms a full fledged Y-junction. The correlation of the carbide forming ability to branch formation was also supported by Y-junction synthesis in Hf-, Zr- and Mo [**194**]-doped Fe catalyst particles [**192**] which also have large ΔH_f (HfC: -26 Kcal/g-atom and ZrC: -23 Kcal/g-atom) It was generally found that the use of Zr and Hf catalysts yield larger diameter Y-junctions.

The ratio of the Ti-precursor gas and the feedstock gases could be adjusted to determine the *growth of the side-branches at specific positions* (Figure 18). For example, a decreased flow of the xylene gas, at a point of time, would halt the growth of the nanotube, while preponderance of the Fe-Ti precursor gas/catalyst particles would nucleate the branch. The Y-junction formation has also been found to be sensitive to temperature, time and catalyst concentration. The optimal temperature range is between 750 – 850 ^{o}C; below 750 ^{o}C, the yield is very low and temperatures greater than 850 ^{o}C produce V-shaped nanotube junctions. Y-junction CNTs with minimal defects, at the junction region, were obtained when the atomic compositions of Fe: Ti: C was in the ratio 1:3:96.

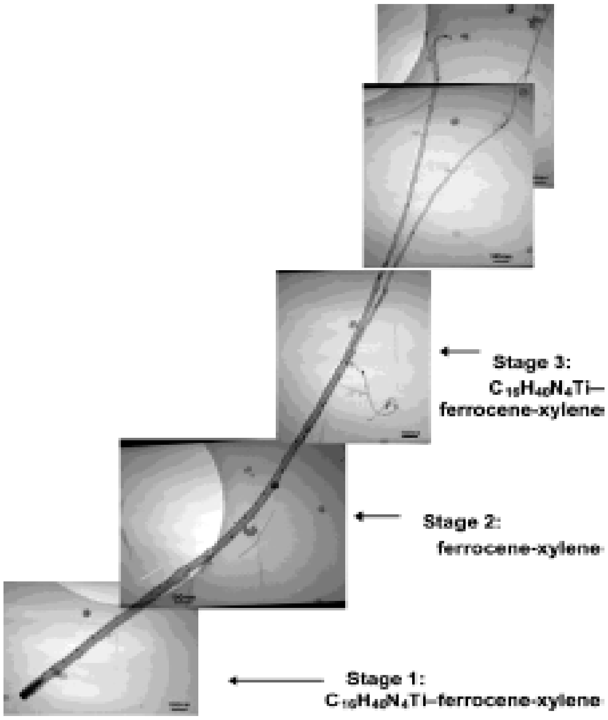

Figure 18. Controlled addition of Ti (see Stage 3) can induce branching in linear nanotubes. Reprinted with permission from Reference [**192**], N. Gothard *et al. Nano Lett*. 4, 213, (2004). Copyright @ The American Chemical Society

The growth of the Y-junctions essentially seems to be a non-equilibrium phenomenon and various other methods have been found to be successful in proliferating branches, such as sudden reduction of temperature during a normal tip growth process [**193**] where over-saturation by the carbon feedstock gas causes a surface energy driven splitting of the catalyst particle and branch nucleation. Other catalyst particles, such as Ca and Si, have also been found to nucleate side branches [**186**]. The location of the junction is in any case a point of structural variation [**190**] the control of which seems to determine the formation of Y-junctions, and its subsequent properties. It should also be possible to undertake a rigorous thermodynamic analysis [**195**] to rationalize the growth of nonlinear forms.

2.3 Electrical Characterization of Y-junction Morphologies

Initial work has focused mainly on the electrical characterization of the nanostructures. In a large part it was motivated by the possible influence of topology on electrical transport, and supported through theoretical predictions on SWNT junctions.

Existing theoretical explanations of electrical behavior in Y-junctions are mainly based on SWNT Y-junctions, and the experimental demonstrations detailed in this paper were made on both SWNT and MWNT Y-junctions [**187**], [**188**]. It is speculated that relatively low temperature CVD methods that have been used to date may not be adequate to reliably produce SWNT based Y-junctions, with larger energetics.

While SWNTs have been extensively studied [**168**], [**196**], MWNTs have been relatively less scrutinized. An extensive characterization of their properties is found in literature [**169**], [**197**]. MWNTs are generally found to be metal-like [**197**] with possibly different chiralities for the constituent nanotubes. Currently, there is some understanding of transport in *straight* MWNTs, where it has been shown that electronic conduction mostly occurs through the outermost wall, [**198**] and inter-layer charge transport in the MWNT is dominated by thermally excited carriers [**199**]. While the outer wall dominates in the low-bias regime (< 50 mV), at higher bias many shells can contribute to the conductance with an average current carrying capacity of 12 μA/shell at room temperature [**181**]. In contrast to SWNTs with μm coherence lengths, the transport in MWNTs is quasi-ballistic [**175**] with mean free paths < 100 nm. Based on the above survey of properties in *straight* MWNTs, we could extend the hypothesis in that non-coherent electronic transport dominates the Y-junctions and other branched morphologies.

2.4 Carrier Transport in Y-junctions: Electron Momentum Engineering

The progenitor of a Y-junction topology, for electronic applications, can be derived from an electron-wave Y-branch switch [**200**] (YBS) where a refractive index change of either branch through electric field modulation can affect switching. This device, demonstrated in the GaAs/AlGaAs [**201**] and InP/InGaAs [**202**], [**203**] based two-dimensional electron gas (2-DEG) system, relies on ballistic transport and was proposed for low power, ultra-fast (THz) signal processing. It was derived theoretically [**183**] and proven experimentally [**204**] that based on the ballistic electron transport, non-linear and diode-like I-V characteristics were possible. These devices based on III-V materials, while providing proof of concept, were fabricated through conventional lithography. It was also shown in 2-DEG geometry [**205**] with artificially constructed defects/barriers, that the defect topology can affect the electron momentum and guide the current to a pre-determined spatial location independent of input current direction. This type of rectification involves a new principle of *electron momentum engineering* in contrast to the well known *band engineering*.

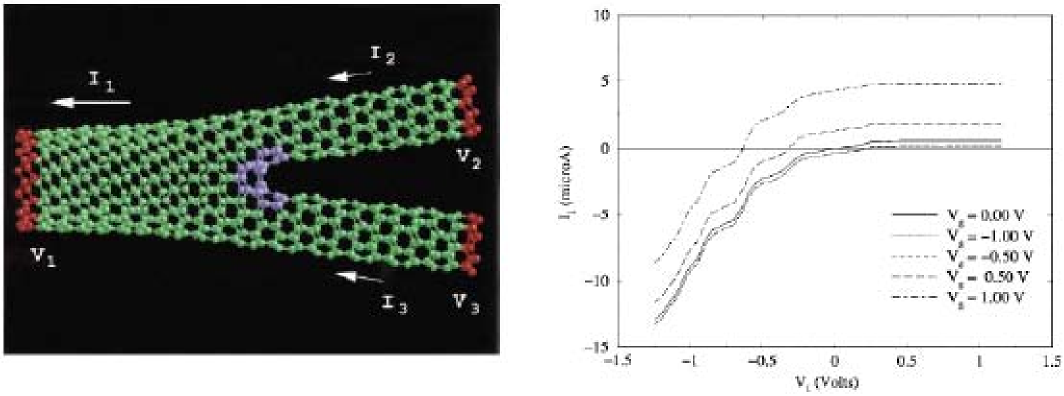

Figure 19. Asymmetry, and rectification like behavior, in the Current-Voltage characteristics of a single walled Y-junction nanotube is indicated, through quantum conductivity calculations. Reprinted with permission from Reference [**206**], A.N. Andriotis *et al. Phys. Rev. Lett.*, 87, 066802 (2001). Copyright @ The American Physical Society.

Nanotubes provide a more natural avenue to explore such rectification behavior. It was theoretically postulated [**206**] that switching and rectification (Figure 19) could be observed in symmetric (*e.g.,* no change in chirality from stem to branch) Y- junction SWNTs, assuming quantum conductivity of electrons, where the rectification could be determined [**207**] by the:

(i) formation of a quantum dot/asymmetric scattering center [**205**] at the location of the Y-junction,

(ii) finite length of the stem and branches connected to metallic leads,

(iii) asymmetry of the bias applied/the potential profile [**208**] across the nanotube, and

(iv) strength of the nanotube-metal lead interactions and influence of the interface [**209**].

Some of the possibilities, where the nature of the individual Y-junction branches determines the electrical transport are illustrated in Figure 20.

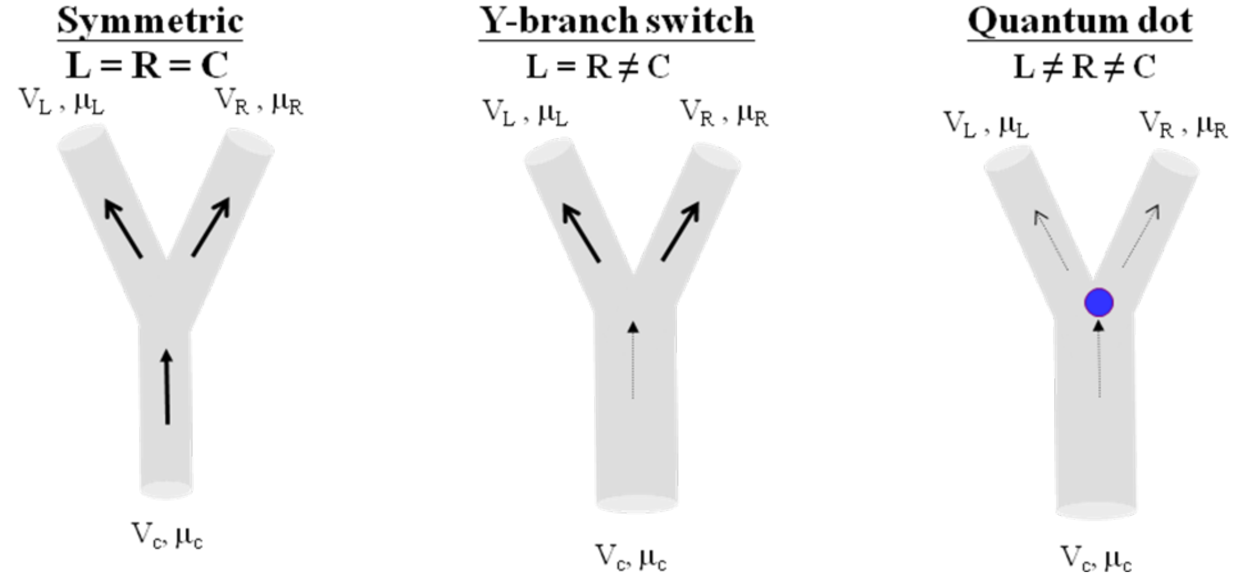

Figure 20. The CNT Y-junction as a prototypical *structural* element for a variety of functions such as switching or as a quantum dot, depending on the characteristics of the individual branches. L, R, and C, refer to the left, right, and central/stem branches of a Y-junction.

2.5 Novel Electronic Functionality of Y-junction Carbon Nanotubes

Generally, the motivation for use of new CNT morphologies, such as Y-junctions, based on either SWNTs or MWNTs, in addition to the miniaturization of electronic circuits, is the possible exploration of new devices and technologies through new physical principles. The existence of negative curvature fullerene based units [**210**], and branching in nanotubes necessitates the presence of topological defects - in the form of pentagons, heptagons and octagons – at the junction regions for maintaining a low energy sp^2 configuration [**211**]. These *intrinsic* defects are natural scattering centers that could affect/modulate the electrical transport characteristics of a nanotube.

At the nanometer scale, the dimensions of the device are also comparable to electron wavelength (λ_F) and electron travel/current must be considered in terms of wave propagation [**212**], analogous to the propagation of light down a optical fiber. Wave phenomena, such as interference and phase shifting, can now be used to construct new types of devices. For example, constructive and destructive interferences can be used to cause transmission and reflection of current leading to switching and transistor like applications with added advantage of very low power dissipation. Novel applications, have been proposed theoretically [**213**], [**214**], [**215**] for ballistic nano-junctions, of which the Y-junction is only one example. Several of these applications have been demonstrated in preliminary experiments and will be elucidated later in the paper. They include:

2.5.1 Switching and Transistor Applications

In a basic Y-junction switch, an electric field can direct electrons into either of two branches, while the other branch is cut off[32]. It has been shown, in computer simulations [**200**], that a sufficient lateral field for electron deflection is created by applying a very small voltage of the order of milli-Volts (mV). The specific advantage of a Y-junction switch is that it does not need single-mode electron waveguides for its operation and can operate over a wide range of electron velocities and energies, the reason being that the electrons are not stopped by a barrier but are only deflected. An operational advantage over a conventional FET could be that the current is switched between two outputs rather than completely turned ON/OFF [**216**], leading to higher efficiency of operation.

An electrical asymmetry can also be induced through structural or chemical means across the two branches in a nanostructured junction. The Y-junction region, for instance, can possess a positive charge[55] due to two reasons, *viz.,* the presence of : (1) topological defects, due to the formation of non-hexagonal polygons at the junction to satisfy the local bond order [**217**], where delocalization of the electrons over an extended area leads to a net positive charge, and (2) catalyst particles, which are inevitably present during synthesis [**192**], [**193**]. This positive charge and the induced asymmetry is analogous to a "gating" action that could be responsible for rectification. While the presence of defects at the junction seems to assist switching, there is also a possibility that such defects may not be needed as some instances of novel switching behavior in Y-junctions are observed in the noticeable absence of catalyst particles. Additional studies are necessary to elucidate this aspect, but such an observation is significant in that a three-dimensional array of Y-junction devices based on CNTs would be much easier to fabricate if a particle is not always required at the junction region.

2.5.2 Rectification and Logic Function

It is possible to design logic circuitry, based on electron wave guiding in Y-junction nanotubes, to perform operations similar to and exceeding the performance of conventional electronic devices [**216**]. When finite voltages are applied to the left and the right branches of a Y-junction, in a push-pull fashion (*i.e.,* $V_{left} = - V_{right}$ or *vice versa*), the voltage output at the stem would have the same sign as the terminal with the lower voltage. This dependence follows from the principle of continuity of electro-chemical potential ($\mu = -eV$) in electron transport through a Y-junction and forms the basis for the realization of an **AND** logic gate, *i.e.,* when either of the branch voltages is negative (say, corresponding to a logic state of 0), the voltage at the stem is negative and positive voltage (logic state of 1) at the stem is obtained only when both the branches are at positive biases. The change of μ is also not completely balanced out due to the scattering at the junction, and results in non-linear interaction of the currents from the left and the right sides [**204**]. To compensate, the resultant center branch voltage (V_S) is always negative and varies parabolically (as V^2) with the applied voltage [**213**].

2.5.3 *Harmonic Generation and Frequency Mixing*

The non-linear interaction of the currents and the V^2 dependence of the output voltage at the junction region also suggest the possibility of higher frequency/harmonic generation. When an AC signal of frequency ω, $V_{L-R} = A \cos [\omega t]$, is applied between the left (L) and right (R) branches of the Y-junction, the output signal from the stem (V_S) would be of the form:

$$V_S = \mathbf{a} + \mathbf{b} \cos [2\omega t] + \mathbf{c} \cos [4\omega t], \text{ where } \mathbf{a}, \mathbf{b} \text{ and } \mathbf{c} \text{ are constants.}$$

The Y-junction can then be used for second and higher harmonic generation or for frequency mixing [**202**]. The second harmonic (2ω) output is orthogonal to the input voltage and can be easily separated out. These devices can also be used for an ultra-sensitive power meter, as the output is linearly proportional to V^2 to very small values of V. A planar CNT Y-junction, with contacts present only at the terminals, suffers from less parasitic effects than a vertical transistor structure and high frequency operation, up to 50 GHz at room temperature [**218**], is possible. It can be seen from the brief discussion above that several novel devices can be constructed on CNT Y-junction technology could be the forerunner of a new paradigm in nanoelectronics.

2.6 Experimental Progress

Compared to the large body of work on electrical transport through linear nanotubes, the characterization of nonlinear nanotubes is still in its infancy. The samples for electrical measurements are typically prepared by suspending nanotube Y-junctions, say, in isopropanol and depositing them on a SiO_2/Si substrate with patterned Au pads. Y-junctions, in proximity to the Au contact pads, are then located at low voltages (< 5 kV) using a Scanning Electron Microscope (SEM) and contacts patterned to each branch of the Y-junction, either through electron-beam lithography [**219**] or focused ion beam induced metal deposition [**220**] – Figure 21. In the latter case, special care needs to be taken to not expose the nanotube to the ion-beam, to prevent radiation damage. The early measurements in Y-junction nanotubes explored the theoretical idea of rectification between any two branches of the Y-junction.

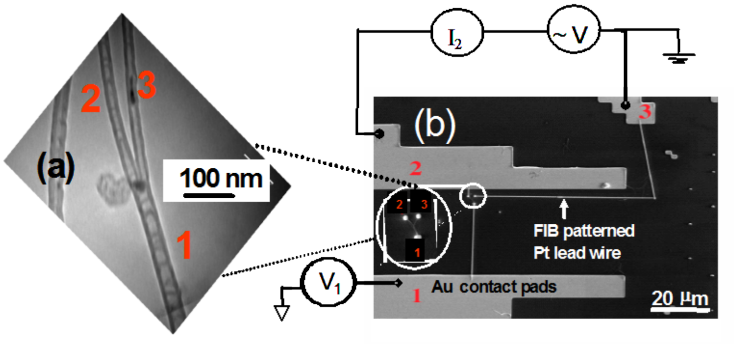

Figure 21. The (a) MWNT Y-junction electrical measurement configuration as imaged in the (b) SEM.

2.6.1 *Rectification Characteristics*

Prab, Initial work in measurement of Current- Voltage (I-V) characteristics of Y-junctions was accomplished through two-terminal measurements using the stem as one terminal and the two branches, connected together, as the other terminal. With a stem/branch diameter ratio approximately 60 nm: 40 nm, diode like behavior was observed [**187**]. The authors ascribing SWNT like p-type semiconductor characteristics, modeled the behavior on a p-p isotype heterojunction where the concentration (*N*) of carriers (holes) varied inversely as the fourth power of the diameter (*D*), i.e., $\frac{N_{stem}}{N_{branch}} \sim (\frac{D_{branch}}{D_{stem}})^4$ The doping mismatch would then presumably account for the rectifying behavior. In the absence of further characterization, it is difficult to see how semiconducting characteristics could be assigned to > 40 nm MWNTs. A subsequent publication from the same group [**221**] ascribed the electrical characteristics to be dominated by activated conduction, presumably through carrier hopping. More complex nonlinear, quasi-diode like behavior has been seen [**8**] in MWNT Y-junctions (Figure 22), which corresponds to a saturation of current at positive bias polarities.

This is predicted from theoretical considerations [**222**] where the current cannot decrease beyond a certain value, but saturates at a value (~ 0.5 μA at positive $V_{1\text{-}2}$) corresponding to the intrinsic potential of the junction region itself. Such behavior has also been seen in Y-junctions fabricated from 2-DEG systems [**204**], [**223**]. The underlying rationale, in more detail, is as follows: the necessity of maintaining a uniform electrochemical potential ($\mu = - eV$) in the overall structure give rise to non-uniform/non-linear interactions [**224**]. For example, when V_2 (the voltage on branch 2) decreases, $\mu_2 (= -eV_2)$ increases, and an excess electron current flows towards the central junction. The balance between the *incoming* current and the *outgoing* currents, at the junction itself, is achieved by increasing μ_1 (decreasing V_1). On the other hand, when μ_2 decreases, μ_1 decreases also, but cannot decrease past a certain critical point, *viz.*, the fixed electrochemical potential, dictated by geometry/defects, of the junction.

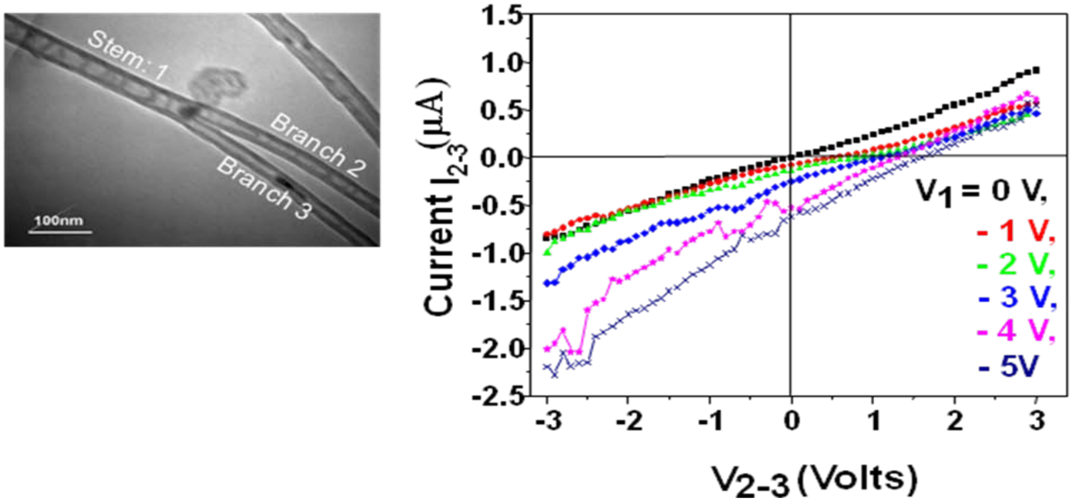

Figure 22. Current (I) – Voltage (V) characteristics of a MWNT Y-junction. A constant d.c. voltage is applied on the stem, while the I-V behavior across branches 2 and 3 are monitored. The gating action of the stem voltage (V_1) and the asymmetric response are to be noted.

Work on SWNT based Y-junctions has revealed the diode like behavior in richer detail. It was established through Raman spectroscopy analyses [**194**] that constituent Y-junction branches could be either metallic/semiconducting. This gives rise to the possibility of forming intrinsic Metal (M) - Semiconductor (S) junctions within/at the Y-junction region. Experiments carried out on SWNTs in the 2-5 nm diameter range [**194**] (which could, depending on the chirality, correspond to either metallic / semiconducting nanotubes with energy gaps in the range of 0.17 – 0.37 eV [**225**] reveal ambipolar behavior where carrier transport due to both electrons and holes could be important. Considering, for example, that the Fermi level (E_F) for the metallic branch of the Y-junction is mid-way the semiconductor branch band gap, positive or negative bias on the semiconductor branch can induce electron/hole tunneling from the metal (Figure 23).

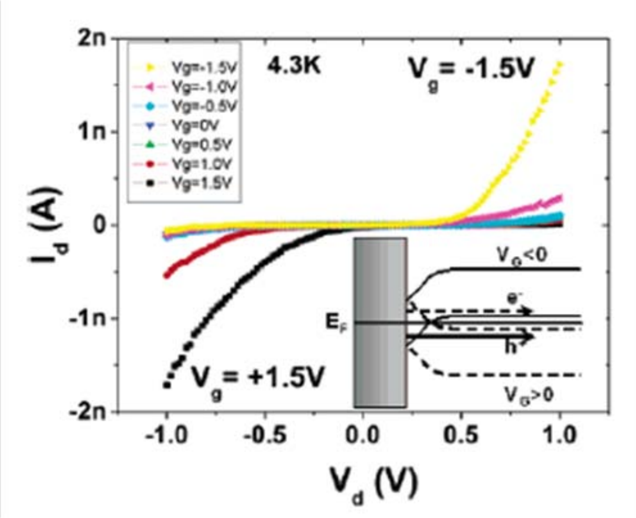

Figure 23. I-V measurements on single walled Y-CNTs, where a metallic CNT interfaces with a semiconducting CNT (see band diagram in inset) indicates ambipolar behavior, as a function of applied gate voltage (on the semiconducting nanotube). Reprinted with permission from Reference [**219**], D-H. Kim *et al. Nano Lett.*, 6, 2821, (2006). Copyright @ The American Chemical Society.

Such temperature independent tunneling behavior was invoked through modeling the I-V characteristics to be of the Fowler-Nordheim type. However, at higher temperatures (> 100 K), thermionic emission corresponding to barrier heights of 0.11 eV could better explain the electrical transport results.

On an interesting note, it should be mentioned that the contact resistance at a branch – metal contact could also play a major role and contribute to the relatively low currents observed in experiments[58]. While MWNTs should theoretically have a resistance smaller than h/e^2 (~ 26 kΩ), ideal, and reproducible, Ohmic contacts, through metal evaporation, have been difficult to achieve.

2.6.2 Electrical Switching Behavior

Intriguing experiments have brought forth the possibility of using the CNT Y-junctions for switching applications as an electrical inverter analogous to earlier [**200**], [**203**], [**204**] Y-switch studies in 2-DEG systems. In this measurement [**8**], a DC voltage was applied on one branch of the Y-junction while the current through the other two-branches was probed under a small AC bias voltage (< 0.1 V). As the DC bias voltage is increased, at a certain point the Y-junction goes from nominally conducting to a “pinched-off” state. This switching behavior was observed for all the three-branches of the Y-junction, at different DC bias voltages.

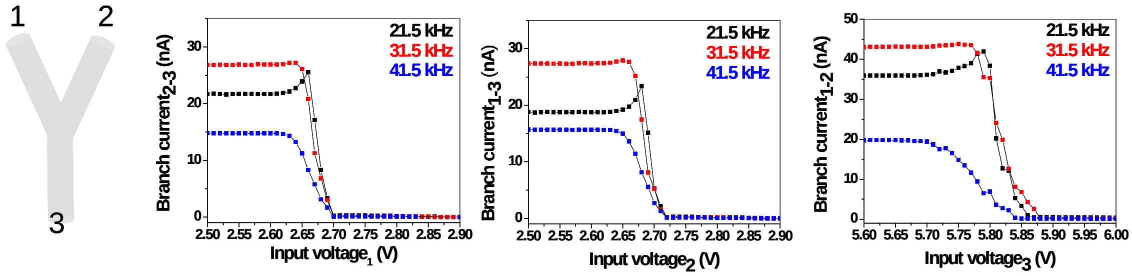

Figure 24. An abrupt modulation of the current through two branches of the Y-junction, indicative of electrical switching, is seen on varying the voltage on the third branch. The voltage, at which the switching action occurs, on the two branches (1 & 2), is similar and smaller (~ 2.7 V, see **a** and **b**) compared to the turn-off voltage (~ 5.8 V) on the stem (3) in **c.** Such abrupt switching characteristics are seen up to 50 kHz, the upper limit arising from the capacitive response of the Y-junction.

The absolute value of the voltage at which the channel is pinched off is similar for two branches (~ 2.7 V, as seen in Figures 24**a, b**), and is different for the third stem branch (~ 5.8 V, as in Figure 24**c**). The switching behavior was seen over a wide range of frequencies, up to 50 kHz, the upper limit being set by the capacitive response of the Y-junction when the branch current tends to zero.

The detailed nature of the electrical switching behavior is *not understood* at present. The presence of catalyst nano-particles (Figure 14) in the conduction paths could blockade current flow, and their charging could account for the abrupt drop-off of the current. The exact magnitude of the switching voltage would then be related to the exact size of the nanoparticle, which suggests the possibility of nano-engineering the Y-junction to get a variety of switching behaviors. However, it was deduced [**226**], through tight binding molecular dynamics simulations on SWNTs, that interference effects could be solely responsible for the switching behavior, even in the absence of catalyst particles. An associated possibility is that there is inter-mixing of the currents in the Y-junction, where the electron transmission is abruptly cut off due to the compensation of currents, for example, the current through branches 2 and 3 is cancelled by current leakage through stem 1. The simultaneous presence of an AC voltage on the source-drain channel and a DC voltage on the control/gate terminal could also result in an abrupt turn-off, due to defect mediated negative capacitance effects [**227**]. Further research is needed to clarify the exact mechanisms in these interesting phenomena.

A suggestion was also made that AND logic gate behavior could be observed [**8**] in a Y-junction geometry. The continuity of the electro-chemical potential from one branch of the CNT Y-junction to another is the basis for this behavior (see Section 2.5.2 for a more detailed explanation).

2.6.3 Current Blocking Behavior

Other interesting characteristics were seen when the CNT Y-morphologies were *in situ* annealed in the ambient, in a range of temperatures 20 – 400^{o}C and I-V curves measured for various configurations of the Y-junction. The observations are summarized in Figure 24 and are fascinating from the point of view of tunability of electrical characteristics. As the annealing is continued, the onset of non-linearity in the I-V characteristics is observed (Figure 24b). With increasing times, the non-linearity increases, but is *limited* to one polarity of the voltage. This is reminiscent of diode-like behavior and can be modeled as such (Figure 24c and inset). With progressive annealing, it was seen that the current is completely cut-off (< 1 pA) and perfect rectification seems to be obtained (Figure 12d) A current rectification ratio ($= \frac{\mathbf{I_{ON}}}{\mathbf{I_{OFF}}}$) of > 10^4 has been calculated, where I_{ON} denotes the current through the Y-device at -3 V while I_{OFF} is the current at + 3 V. The transition to linear characteristics was more rapid at elevated temperatures of annealing (> 200 ^{o}C). In yet another set of Y-junction samples reversible behavior from Ohmic to blocking type was observed (Figure 25). Interestingly, it was observed that the current through one set of branches (S1-B3 in Figure 26b) was not affected by the annealing, while the blocking voltages differ for the other two configurations (viz., ~ 0.1 V for S1-B2 and ~ 2.6 V for B2-B3).

The time-dependent behavior and rectification seems to be both a function of temperature and time of annealing. The sharp cut-off of the current at positive voltages is also remarkable (the cut-off of the currents at the positive polarity of the voltage seems to be indicative of hole transport in the Y-junctions, through electrostatic doping, due to the work function of Pt, ϕ_{Pt} ~ 5.7 eV being larger than ϕ_{CNT}). While it is well known that contacts to p-type CNTs through high work-function metals, where $\phi_M > \phi_{CNT}$ (~ 4.9 eV) result in Ohmic conduction [**101**], [**228**], the transition from conducting to blocking behavior is generally more gradual. A continuous change in the current was also seen when a gate voltage modulates the p-CNT channel conduction and in CNT based p-n junctions with diode-like behavior [**228**], [**229**], [**230**]. Consequently, we think that the observed behavior is unique to the CNT branched topologies examined here.

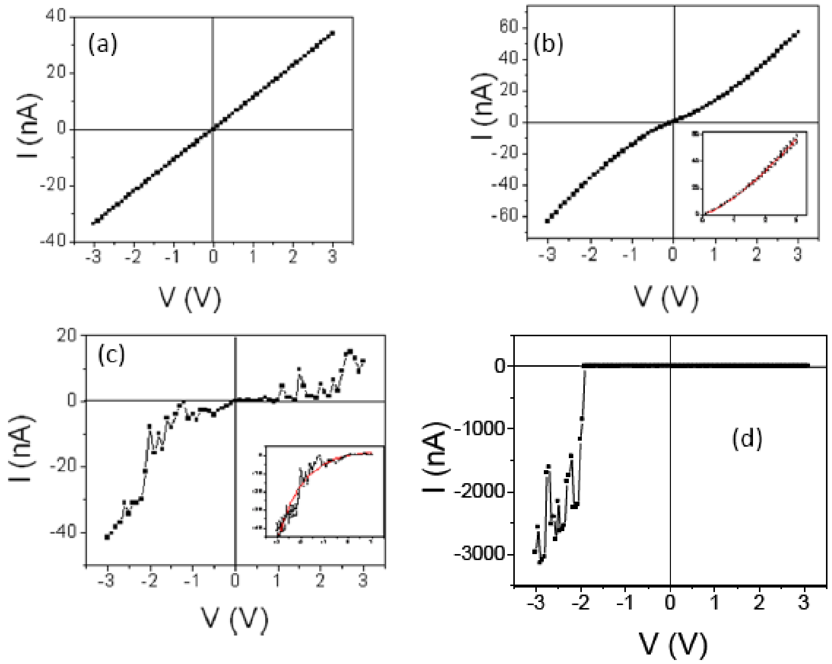

Figure 24. The I-V characteristics for a CNT Y-junction subject to high temperature annealing (~ 150 °C) as a function of annealing time, *after* being cooled down to room temperature. (a) Prior to annealing Ohmic behavior is observed. At increasing times non-linearity is introduced (b) which can be modeled in terms of space charge currents (see inset) as I = A V + B $V^{3/2}$. Further annealing results in a (c) diode-like behavior (the inset shows a fit: $I = I_o\,(e^{(\frac{eV}{k_B T})} - 1)$ and finally in a (d) current-blocking/ rectification behavior where a 10^4 fold suppression in current is seen.

The annealing induced rectification behavior in Carbon Nanotube (CNT) Y-junctions could be intrinsic to the Y-nanotube form or be related to the nature of the contacts. It was reported that SWNTs contacted by

Pt [**101**] could yield non-metallic behavior, arising from a discontinuous [**231**]contact layer to the nanotubes. It is also possible that the outer contacting walls of the MWNT (multi-walled nanotube) Y-junction are affected by the annealing procedure, resulting in a modification of the Schottky barrier [**96**]. Several CNT device characteristics, such as transistors [**232**]and photodetectors [**233**]are Schottky barrier mediated. Exposure to oxygen is also known to affect the density of states of CNTs and the I-V characteristics [**96**] However, the low temperatures (< 300°C) employed in the experiment precludes oxidation [**181**], [**234**] and the blocking behavior that were observe in our experiment cannot be justified on the above principles.

A hint for explaining this intriguing I-V behavior is obtained through modeling the I-V characteristics of Figure 24b), an intermediate stage in the annealing process. A supra-linear behavior, *viz.*, **I** proportional to A**V** + B$\mathbf{V}^{3/2}$, can be fitted (Figure 24b inset) which could be indicative of space-charge limited currents (A and B are numerical constants). To further understand the transport behavior, it becomes necessary to examine the role of the contacts in detail. Prior to annealing, where we observe linear behavior (Figure 24a), i.e., the Ohmic contact is a reservoir of free holes. Generally, the ratio of the hole transit time (t_{tr}) to the dielectric relaxation time (t_{rel}) in the CNT determines the carrier dynamics and currents. A large (t_{tr}/t_{rel}) ratio, obtained, say at smaller voltages would result in Ohmic currents while a lower (t_{tr}/t_{rel}) ratio, at increased voltages, would imply space charge currents (Figure 25c). As t_{rel} is inversely proportional [**235**] to the conductivity (σ), such effects would be more important at elevated temperatures for metallic Y-CNTs.

We suggest then that the saturation of the current at positive voltages could be due to space charge effects. In other words, at sufficiently high voltages (> 0.1 V for S1-B2 and > 2.6 V for B2-B3 in Figure 25b), further hole generation is choked due to preponderance of space charge and negligible current is observed. Note that such a scenario can also be predicted from the band structure diagrams at the metal contact-CNT interface (Figure 26). Here, at (ii) forward bias, there is a significant barrier to hole transport and space charge processes could be important. At (iii) negative voltages, however, no hole barriers exist and Ohmic conduction is obtained. The space charge hypothesis is also supported by the observation that over a period of time, the blocking behavior reverts to Ohmic conduction. In an earlier study [**236**] of a straight SWNT diode containing a charged impurity, similar space charge based arguments were invoked to explain the observed current rectification. We are currently conducting experiments to probe the time constants and dynamics of current flow through the Y-CNTs.

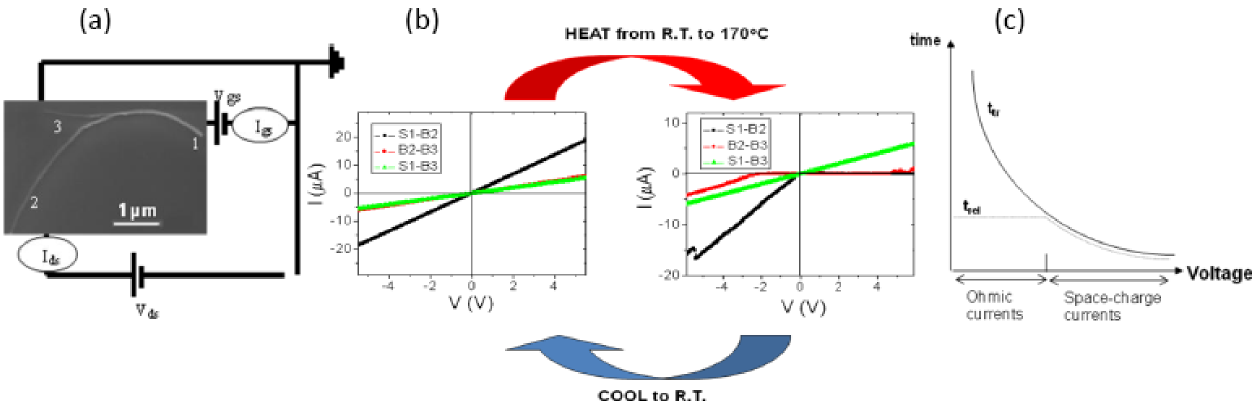

Figure 25. **(a)** Circuit arrangement used to probe the current (I)-voltage (V) characteristics of Y-CNT (SEM micrograph). **(b)** Reversible current blocking behavior induced in the CNT Y-junction. The individual segments' electrical transport characteristics exhibit different blocking/linear characteristics and are geometry dependent. **(c)** The transition from Ohmic behavior to space charge behavior is a function of voltage and can be accelerated at higher temperatures. The ratio of the transit time (t_{tr}) to the dielectric relaxation time (t_{rel}) determines the dynamics of the carrier transport.

We speculate that the *different diameters* of the branches of the Y-junction (Figure 14 or Figure 25a) could be playing a role in the current blocking behavior. The basis is the observation (Figure 25b), where rectification is not observed for a particular (S1-B3) two-terminal configuration. It was found that the magnitude of the conductance (g_d) between any two terminals of the Y-junction is *inversely* proportional to the ratio of the diameters through which the current is flowing (see Figure 25b), *i.e.,* a larger discrepancy between the branch diameters lowers the conductance. In analogy to fluid flow through a pipe, the hole current can similarly be modulated by the Y-junction geometry. It would be instructive to characterize the blocking behavior systematically as a function of branch diameters in the Y-junction geometry.

The phenomena of current being low when the voltage was high, in terms of space charge distribution was noted by Shockley [**237**], who remarked on its presence in the collector region of a junction transistor amplifier. The I-V characteristics observed in the CNT Y-forms here could be compared to that of a transit-time device such as an BARITT (Barrier Injection and Transit Time) diode [**238**]. Such devices consider space charge limited currents for creating *negative resistance* regions which can be exploited for switching, oscillation, amplification and other functions in high-speed circuitry [**239**]. The time delay associated with space charge dissipation is useful for generating microwaves and the BARITT devices are consequently used as local oscillators in microwave receivers.

2.6.4 *Metallic Y-junctions*

It is also possible that the constituent nanotubes in the Y-junction can exhibit metallic conduction, in which case the behavior is analogous to that of three interconnected metal lines! Such behavior has indeed been observed [**240**] . The notable features are: (a) Ohmic conduction, (b) a proportional displacement of the current with V_{gs} and V_{ds}, and (c) a geometry dependent conductance. It was found that the magnitude of the *output conductance,* $\mathbf{g_d} = \left(\frac{\partial I_{ds}}{\partial V_{ds}}\right)_{V_{gs}}$, the ratio of the output current to the bias voltage at a constant gate voltage, is *inversely* proportional to the ratio of the diameters of the branches through which the current is flowing, *i.e.,* a larger discrepancy between the branch diameters lowers the conductance. On the other hand, the $\mathbf{g_m}$, which denotes the gating efficiency for current modulation, seems to be *directly* proportional to the diameter of the gating nanotube [**240**].

It was also suggested that other interesting applications could be facilitated by such experimental results and observations. For example, a single Y-CNT switching device can be made to have diverse operating characteristics through the use of different gating terminals. Y-junction based technology can be used for devices with (1) multiple programmable characteristics, and as (2) components in Field Programmable Gate Arrays (FPGAs) for reconfigurable computing [**241**], where it would be possible to dynamically alter circuit paths. The large scale integration density and high speed of signal propagation intrinsic to nanotubes would be advantageous in this regard.

2.7 Topics for Further Investigation

For the novel applications of Y-CNTs to be practicable, it would be important and necessary to gain better control of the geometry, through synthesis or processing, of Y-CNTs. It is plausible that remarkable features of Y-junction based transistors such as the abrupt switching [**8**] and differential gain [**221**] observed in earlier studies could be related to the presence and location of defects. *In situ* engineering of CNT morphology, e.g., exposure to intense electron-beam radiation [**185**] could also be utilized to tailor individual Y-CNT characteristics. Other aspects that merit further study include:

(a) Characterization of the detailed morphology of the Y-junctions and their effect on the electrical properties. Catalyst particles have been found both at the junction, along the length of the Y-junctions and at the tips [**186**] (Figure 1). The effect of the location, type, and composition of these particles and their scattering characteristics on the electrical transport would yield insight into their influence.

(b) Detailed study of the growth mechanisms of multi-junction carbon nanotubes vis-à-vis the influence of the catalyst particles. It has been contended [**193**] that a perturbation during growth could promote the formation of branches/junctions. For example, if the temperature is reduced during the growth process, a catalyst particle over-saturated with carbon can be induced to nucleate another branch. On the other hand, if the Ti catalyst does play a role, the importance of carbide formers in inducing side-branch growth is interesting from a basic thermodynamic point of view, *i.e.,* is a high negative heat of formation (ΔH_f) of the carbide formers necessary? It is worth noting that Y-junctions and other morphologies, such as H-junctions and T-junctions [**190**], are also formed when methane (which could yield positive ΔH_f) is used as a precursor. The composition of the catalyst particle, which nucleates the nanotube branches [**193**], and the effects of stress generated at the growing nanotube tips could also be playing important roles [**190**] in Y-junction growth.

(c) The issue of electrical conductivity through nanotubes with bends, junctions, and catalyst particles which is also important for the future viability of nanotube based electronics. While the MWNT has an intrinsic resistance, say due to ballistic transport, a capacitive and inductive component will also have to be considered due to the presence of particles, inter-tube transport *etc.* Such a study will also yield insight into the speed of operation of the nanotube based devices and affecting factors, - in terms of the RC delay. It has been theoretically proposed [**242**] that *straight* SWNTs are capable of THz operation and can even be used as nano-antennae [**243**] for radiation and detection in these very high frequency ranges. Whether SWNT or MWNT Y-junctions are capable of being operated at such high frequencies, due to the presence of defects, and determining an ultimate limit [**244**] to their performance is worth investigating.

(d) It has been proposed [**245**], that novel CNT based circuits based on Y-junctions and branched morphologies can be created. These circuits could be fabricated so as to construct universal logic gates such as NAND/X-NOR. Such a demonstration together with the possibility of multi-functionality, *e.g.,* where the catalyst particle could be used for photon detection [**246**] will be important. A variety of such novel circuits can be fabricated leading to a potentially new paradigm for nanoelectronics that goes well beyond traditional FET architectures-*shape controlled logic elements*.

(e) Assembly into a viable circuit topology and large scale fabrication are issues that are of paramount importance. Currently, the Y-junctions are grown in mats/bundles and individually isolated and measured. A scheme where each junction is assembled in this way is not viable practically. Ideas into self-assembly and controlled placement [**247**] of nanotubes will have to be addressed. While some measure of success has been achieved in coordinating the placement of loose nanotubes, *e.g.,* through the use of chemically functionalized substrates [**248**] along with dip-pen lithography [**249**], an orienting electric field-exploiting the nanotubes' dipole character [**79**], through magnetic field [**173**], and microfluidic arrangements [**250**], assembly of such loose nanotubes is difficult to scale up and still remains a critical issue. An array of Y-junctions can be prepared on the same nanotube stem, as was found in preliminary studies, by exposing only periodic locations [**251**] along the length of a nanotube, sputter depositing catalyst, and growing parallel Y-junction branches from these linear array of catalysts using electric field induced direction control during subsequent CVD process, *e.g.,* at any angle from the main stem. The above growth technique could be used to make multiple Y-junction devices in series/parallel. This proof of growth will go a long way in demonstrating the feasibility of large scale nanoelectronic device assembly – a question of the highest importance in recent times.

The study of Y-junctions is still in its infancy. Their synthesis, while reasonably reproducible, is still challenging in terms of precise placement on a large scale- it is worth mentioning that this is an issue even with linear nanotubes and might well determine the feasibility of CNT applications. Presently, both single walled and multi-walled Y-CNTs, the constituent branches of which could have different diameters or semiconducting/metallic character, have been synthesized. Such internal diversity gives rise to novel phenomena such as (1) rectification/current blocking behavior, (2) electrical switching and (3) logic gate characteristics. It is also interesting to investigate whether the three terminals of the Y-CNT can be interfaced into a transistor like paradigm. Future investigations should correlate detailed physical structure of the nanostructure morphologies to the electrical measurements to gain a better understanding of the conduction processes vis-à-vis the role of defects and geometry in non-linear structures. Such a comprehensive and correlated study would be useful to the nanotube/nanowire community and pave the way to the realization of *shape controlled* nanoelectronic devices exclusive to the nanoscale.

3.0 Quasi-1D Graphene Nanoribbons

3.1 Introduction

The 1D forms of carbon discussed thus far, such as SWNTs, MWNTs, CNFs, and Y-junctions, are derivatives of graphene's 2D honeycomb lattice. The electronic structure and properties of graphene have been analyzed theoretically since the 1940s [**252**]. Free standing, atomic monolayers of 2D graphene were discovered in the laboratory by Gheim and co-workers in 2004 by mechanically cleaving a sample of graphite [**21**]. This discovery and the experimentally measured properties of graphene suggest that it has remarkable prospects for technological applications. Up until graphene's recent discovery in the laboratory, 2D atomic monolayers were presumed to generally exist only as parts of larger 3D structures, such as epitaxially grown crystals on lattice-matched substrates [**253**]. Without such a 3D base, theory predicted that 2D monolayers were thermodynamically unstable [**254**] and presumed not to exist naturally. Since the empirical synthesis of graphene, other free-standing 2D atomic crystals have been synthesized, such as single layer boron nitride (BN) and half layer bismuth-strontium-calcium-copper-oxide (BSCCO) [**255**].

The 2D crystals in graphene are not only continuous over length scales of 100's of μm, but they also exhibit a high-degree of crystallinity as evidenced from the exceptionally high electron mobility and ballistic electronic transport in graphene. Moreover, the electrons in graphene interact with the honeycomb lattice in a remarkable way. Such charge carriers are referred to as massless Dirac fermions, where the electrons move relativistically at speeds of ~ 10^6 ms^{-1} instead of 3 x 10^8 ms^{-1} [**252**]. These unique physical attributes make graphene a remarkable platform in which to also examine relativistic and interesting low-dimensional physics effects, besides the obvious potential it has for technological applications [**256**].

A critical element in the realization that graphene had been formed came about by placing the crystallites on the right substrate, which makes a single sheet visible in an ordinary optical microscope. If the graphene sheet is placed on a 300 nm thick SiO_2 layer on a Si substrate, interference effects between the graphene and the SiO_2 layer arise which lead to contrast differences and makes graphene visible using an optical microscope. However, if a thickness difference in the SiO_2 layer as small as 5% arises, (e.g. 315 nm instead of 300 nm), it can make a single sheet of the crystal completely invisible. Since its initial discovery, such a simple technique has proven invaluable to effectively and quickly scan the substrate for graphene crystallites. Recently, Raman microscopy has also been used to identify graphene, which also provides an effective means to evaluate thickness [**257**].

Although electronic transport in graphene can be ballistic, its predominantly metallic character is somewhat limiting for its application as transistor elements in logic gates for example. Approaches have been devised recently where semiconducting energy gaps were engineered in graphene, which opens a potential pathway for its application in semiconducting devices and circuits. One such approach employs quasi-1D graphene nanoribbons (GNRs) which are narrow strips of graphene with widths < 10 nm. The boundary conditions on the edges spatially confine the electrons, inducing band-gaps in the narrow strips of monolayer thick graphene [**258**]. The band gaps which arise in the GNRs are sufficiently large to be useful for room temperature transistor operation, with the added benefits of high switching speed, high carrier mobility and ballistic transport [**21**]. It is interesting to note that the band gaps in GNRs can be engineered on demand, which differs from SWNTs for example, where 2/3 are semiconducting as a result of the CVD synthesis process.

In Section 3.2.1 and Section 3.2.2, the electronic and mechanical properties of graphene and GNRs will be discussed in more detail, which is followed in Section 3.3 with a description of the synthesis techniques for graphene and GNRs. Finally, the transistor applications of GNRs are discussed in Section 3.4.

3.2 Physical Properties of Graphene and Graphene-Nanoribbons (GNRs)

3.2.1 Electrical properties

A single layer of graphene was shown to have a band structure characteristic of a zero-gap semiconductor or semi-metal. The structure becomes increasingly more complicated when three or more graphene layers are stacked on top of each other; the band structure can serve as a practical means to distinguish single, double, and few (3-10) layer graphene which represent three different types of 2D graphene crystals [**259**]. When 10 or more layers of graphene are stacked together, the electronic structure and properties of this configuration resemble bulk 3D graphite [**260**].

The high mobility of the charge carriers in graphene is an attractive feature for its application in high-frequency electronics. In typical metals, impurities in the metal scatter the electrons, which leads to energy dissipation and the onset of electrical resistance. In contrast, graphene's electrical conductivity is not effected by impurities or chemical dopants [**261**], which enables the electrons to traverse many microns without scattering. Such exceptional electronic transport characteristics make graphene a promising material for the realization of a ballistic transistor, potentially operable at room temperature. In addition, a large value of the Fermi velocity and low resistance contacts without a potential Schottky barrier, such as that encountered with CNTs, should enable small switching times and facilitate the demonstration of transistors operational at high frequencies (e.g. THz).

The measured carrier mobilities in graphene directly on SiO_2 substrate routinely reach ~ 10, 000 $cm^2V^{-1}s^{-1}$ [**21**]. It is believed that scattering from external sources, such as scattering centers from the graphene-substrate interface, are the primary limiting factors for electronic transport in unsuspended graphene samples. Prior attempts have been made to remove the substrate to yield free-standing graphene over a trench [**262**], [**263**]. Bolotin *et al.* [**264**] recently fabricated suspended graphene sheets which had multiple electrical contacts, as shown in Fig. 26, which were used to ascertain the inherent electrical properties of graphene, independent of the substrate. Although the electron mobility of such suspended graphene sheets was found to be higher, ~ 28, 000 $cm^2V^{-1}s^{-1}$, these values were comparable to the best reported mobilities for unsuspended devices, suggesting that scattering was not dramatically reduced by the removal of the substrate. However, upon current annealing the devices, mobilities on the order of ~230,000 $cm^2V^{-1}s^{-1}$ were observed, indicative of ballistic transport over μm length scales [**264**]. It is postulated that electrical current annealing removes adsorbed impurities from the graphene-SiO_2 interface by locally heating the surface, where the temperatures reach ~ 600°C.

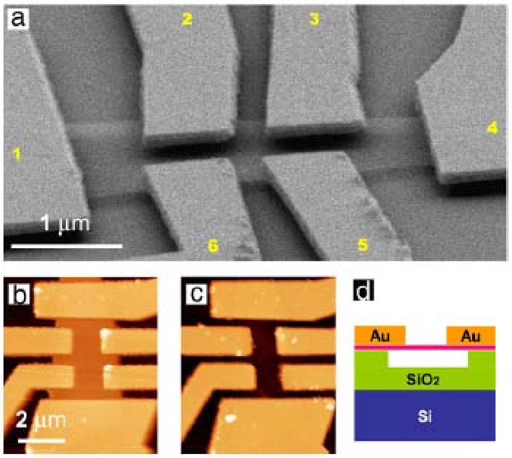

Figure 26. (a) A graphene sheet which is suspended and is contacted at 6 points, as shown, in order to make electrical transport measurements to determine parameters such as mobility. AFM image of the suspended sheet (b) before and (c) after exposure to an oxygen plasma which removed the graphene. (d) Cross sectional schematic of the device where a degenerately dope Si is used as the gate; Au/Cr electrodes are used as the electrical contacts. Reprinted from Reference [**264**], *Solid State Communications* **146**, K. I. Bolotin *et al.*, Ultrahigh electron mobility in suspended graphene, 351, Copyright 2008, with permission from Elsevier.

Beside the prospects for high mobility and ballistic transport, it is important that graphene exhibit a finite band gap so it is useful for transistor applications. Several approaches have been used to accomplish this. First, when a perpendicular electric-field is applied to two-layer graphene, a band gap of ~ 10 meV is induced using a double-gate configuration; however, the band-gaps induced in this manner appear to be relatively small, preventing their applicability for room temperature FETs [**265**]. While larger gaps are possible using NH_3 adsorption on graphene which serves as an electron donor for back-gated bilayers, such an approach is not practical due to the use of NH_3 [**266**]. A band gap in graphene can also arise by using GNRs, which are another quasi 1D form of carbon besides SWNTs or MWNTs. Theory predicts that the crystallographic orientation in GNRs determines whether or not it has a finite energy gap [**258**]. For ribbon widths below ~ 20 nm, the energy gap ΔE in a GNR is expected to scale with ribbon width W, according to $\Delta E = 2\pi\hbar v_F / 3W$ [**258**], [**267**]. The experimentally observed scaling of ΔE with W was confirmed by Han *et al.*, who demonstrated ΔE ~ 200 meV for GNRs with W ~ 15 nm, as indicated in Fig. 27 [**25**]. While theory predicts that ΔE depends sensitively on the boundary conditions at the edges (e.g. if the edges are zig-zag or arm-chair), such a dependence on crystallographic orientation has not been observed experimentally. This is primarily from the difficulty in controlling fabrication processes sufficiently to practically yield smooth edges with a selective crystallographic orientation [**25**].

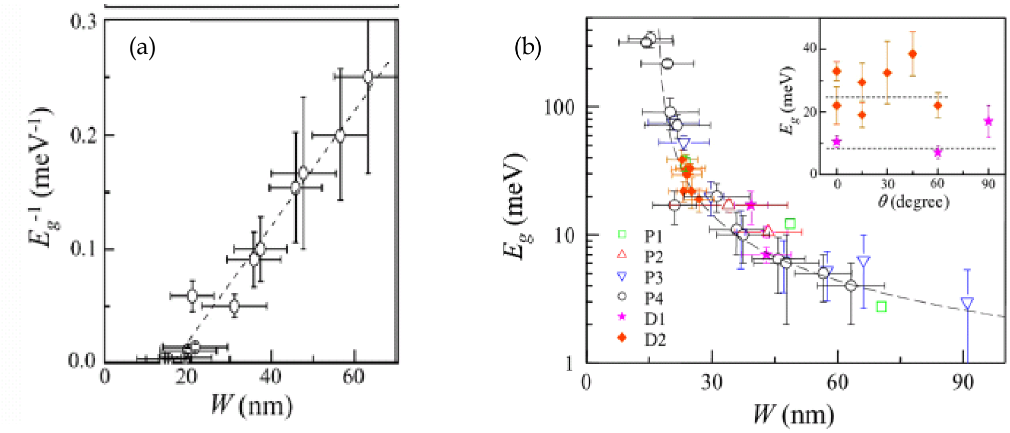

Figure 27. (a) and (b) show the scaling of band-gap E_g as a function of the GNR width, which indicate that the band-gaps in GNRs can be engineered. Reprinted with permission from Reference [**25**], M. Han, *et al.*, *Phys. Rev. Lett.* **98**, 206805 (2007). Copyright 2007 by the American Physical Society.

Interestingly, band gaps arising from other types of mechanisms have been observed in graphene, such as those associated with the Josephson effect [**268**], where supercurrents supported by graphene were carried by Dirac fermions. In this case, electrical contacts to single and few layer graphene sheets were made using superconducting Ti/Al as shown in Fig. 28; when these devices were cooled below the critical temperature of the electrodes (T_c ~ 1.3 K), supercurrents on the order of 100 – 200 nA were measured via the graphene layer through the proximity effect [**269**]. The measured energy gap Δ was ~ 125 μeV, consistent with the Ti/Au bilayers, as indicated by the data in Fig. 29. A Fraunhaufer interference pattern was also observed (Fig. 29b) and demonstrates that the Josephson effect in graphene is robust and intimately linked to graphene's unique electronic structure, which may be useful for low-temperature electronics applications.

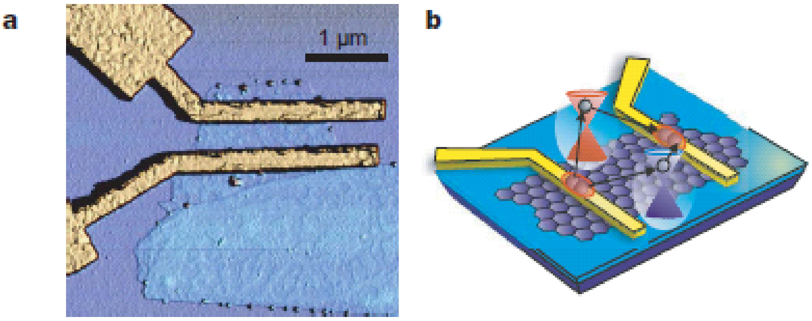

Figure 28. (a) A single graphene layer is contacted with Ti/Al electrodes, as indicated by the AFM image where electrode separations were 100 – 500 nm. (b) Schematic representation of graphene between superconducting electrodes showing the two electrons of the cooper pairs. Reprinted by permission from Macmillan Publishers Ltd: Nature, Reference [**269**], copyright 2007.

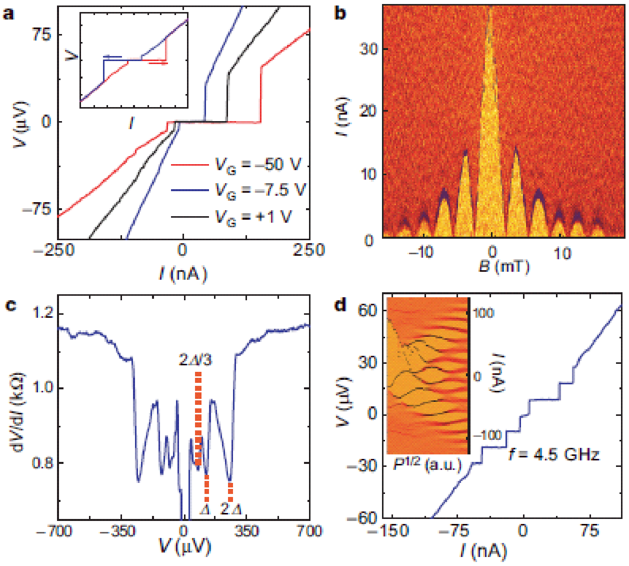

Figure 29. (a) An I-V characteristic showing the Josephson effect in graphene, where a critical current is measured at 0 V. (b) Measurements which show the Fraunhofer-like pattern with the graphene barrier layer. (c) The differential resistance, dV/dI as a function of voltage which shows multiple Andreev reflections dips below the superconducting energy gap Δ. (d) The a.c. Josephson effect, showing the Shapiro steps when microwave radiation at 4.5 GHz is applied to the devices in the graphene-based superconducting devices. Reprinted by permission from Macmillan Publishers Ltd: Nature, Reference [**269**], copyright 2007.

3.2.2 Mechanical Properties

Many of the measurements performed on graphene thus far have primarily focused on determining its electronic properties. The mechanical properties of monolayer thick graphene has also been explored recently which has implications for its applicability to NEMS. Nanoindentation with an AFM tip has been used to measure the mechanical properties of monolayer graphene membranes suspended over wells that were lithographically defined over diameters as large as 5 mm x 5 mm (Fig. 30) [**270**]. These measurements yielded a Young's modulus E = 1 TPa over a wide range of samples as the histogram in Fig. 30e indicates. The sp^2 nature of the bonding in graphene renders it very strong, and explains the large magnitude of the modulus similar to what has been observed with CNTs.

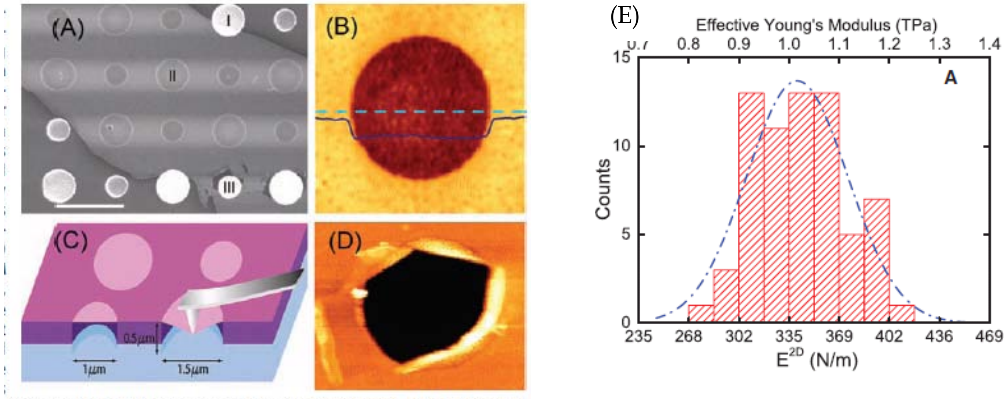

Figure 30. Mechanical measurements on suspended graphene membranes. (A) SEM of arrays of suspended graphene sheets over vias of various sizes. (B) An AFM image of one membrane in the non-contact mode. (C) A schematic of nanoindentation on suspended graphene membrane showing the AFM tip contacting the central region of the suspended graphene sheet. (D) A fractured membrane after the mechanical measurements. (E) A histogram of the measured Young's modulus which yields values ~ 1 TPa for graphene. From Reference [**270**]. Reprinted with permission from AAAS.

Monolayer thick graphene, as well as multilayer graphene sheets have been applied for mechanical resonators, where the graphene-based membranes were suspended over trenches [**263**]. A schematic of such a structure is illustrated in Fig. 31a, where an electrostatic driving mechanism is shown. Besides electrostatic actuation, optical actuation was also used where the intensity of a diode laser was used to periodically expand and contract the graphene, and the motion was subsequently detected by a fast photodiode. Some resonance measurement results are shown in Fig. 31c - d, and Qs ranging from ~ 20 to 850 have been measured with the zeroth-order resonance frequency f_0 ~ 1 MHz to 170 MHz. In addition, the graphene resonators showed no degradation in Young's modulus with decreasing thickness in contrast to what is typically observed with ultrathin Si cantilevers.

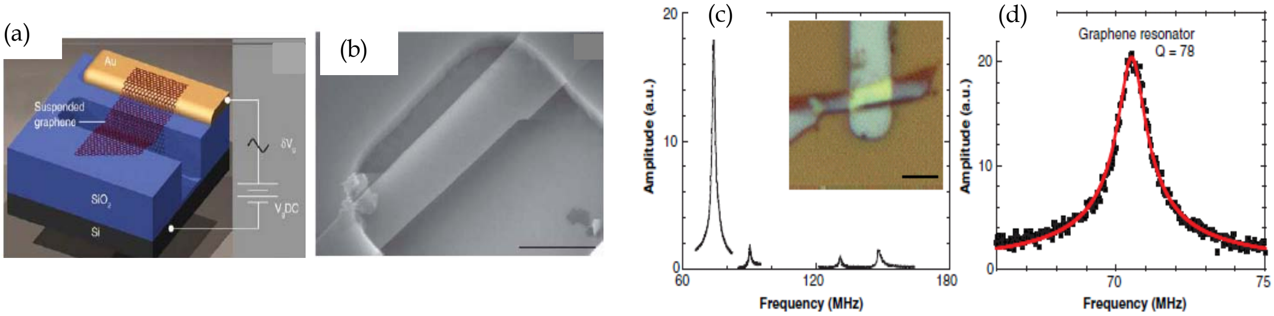

Figure 31. (a) An illustration showing a suspended graphene resonator which is actuated electrostatically. (b) An optical image of graphene suspended over a trench; the graphene is ~ 4 layers thick. (c) Optical resonator measurements of 15 nm thick graphene (in the inset) showing amplitude versus frequency. Scale bar, 5 mm. (d) Resonance measurements on single-layer graphene indicating a resonance frequency of ~ 71 MHz for the first-order mode and a Q ~ 78. From Reference [**263**]. Reprinted with permission from AAAS.

Theoretical calculations on the mechanical properties of quasi-1D GNRs have also been initiated recently for a large set of hydrogen-terminated GNRs with varying lengths and widths [**271**]. The effect of uniaxial strain on the electronic properties of infinite GNRs has also been analyzed in detail [**272**]. The electromechanical properties of suspended GNRs under bending and torsional deformations, yielded a Young's Modulus of ~ 7 TPa [**271**], making quasi-1D GNRs one of the strongest materials known to man.

3.3 Formation of Graphene and Graphene-Nanoribbons (GNRs)

Mechanical exfoliation from 3D bulk graphite was the first approach used to yield isolated, monolayer thick graphene for the first time [**21**], and this technique has been used in subsequent investigations to further characterize the physical properties of graphene [**255**], [**256**], [**257**], [**262**], [**273**]. A commercialized process [**274**] has also emerged where mechanical exfoliation of highly-oriented pyrolytic graphite (HOPG) is used for the formation of graphene, but this technique is slow and yields few μm flakes per square-cm. Other approaches have also been attempted in order to yield monolayer or few-layer thick graphene sheets. In Section 3.3.1, chemical synthesis and bottom-up approaches used for forming graphene and GNRs will be discussed, while in Section 3.3.2 the use of top-down approaches for forming GNRs is described.

3.3.1 Chemical Synthesis and Bottom-up Approaches

The oxide on exfoliated graphite oxide has been reduced using chemical approaches to synthesize graphene [**275**], [**276**], [**277**]. Graphene has also been synthesized epitaxially involving the vacuum graphitization of SiC substrates [**278**], [**279**]. Although the use of SiC substrates may be suitable for the large-scale production of graphene potentially for industrial applications, various lattice scale defects have been observed with these approaches, which leads to scattering [**280**].

Recently, metal substrates have also been employed to synthesize graphene by the catalytic decomposition of hydrocarbons on metal substrates [**281**], [**282**]. Some of the metals that have been used as templates include Co(0001), Ni(111), Pt(111), Pd(111), Ru(0001), or Ir(111). In particular, very low defect densities have been observed when low-pressure (LP) CVD of ethylene was used to synthesize monolayer thick flaxes of graphene on Ir(111) substrates at temperatures in excess of 800ºC [**281**]. After graphene is synthesized, Raman spectroscopy can also be used to identify the position and intensity of the G peak (at ~ 1580 cm^{-1}) Although significant progress has been made in the chemical and bottom-up synthesis of graphene, more work is still required in order to produce graphene monolayers over extended length scales.

3.3.2 Top-down Approaches for Forming Graphene-nanoribbons

When charge carriers in graphene are confined in the lateral dimension by the formation of quasi-1D GNRs, numerous theoretical reports suggest that a band gap should emerge which is predicted to depend on the width, as well as the specific crystallographic orientation of the ribbon [**258**], [**283**], [**284**], [**285**], [**286**]. GNRs with zig-zag shaped edges are presumed to have direct band gaps, where the band gap decreases with increasing width, while arm-chair shaped edges can be either metallic or semiconducting depending on their widths. Opening band gaps in GNRs is thus very important for transistor applications, and the planar configuration of graphene makes it very compatible with existing device Si IC technology.

In order to form band gaps which are large enough for room temperature operation, the widths of the GNRs need to be less than ~ 10 nm. Present generation nanolithography techniques derived from the Si microelectronics industry have progressed significantly which make the realization of such feature sizes possible. There are already reports where GNRs with widths as low as few nm have been fabricated using top-down techniques [**287**], [**288**]. However, it has been difficult to achieve smooth edges in these structures [**25**] where roughness < 5 nm is necessary to minimize scattering occurring at the edges which limits the ON/OFF ratios in the transistor applications of such devices [**287**]. Techniques need to be devised where etching can selectively control the crystallographic orientation of the GNRs at the edges, for example producing zig-zag or arm-chair terminated edges on demand.

Recently, there have been reports where chemical reactivity differences between zig-zag and arm-chair edges have led to the formation GNRs with ultra-smooth edges (~ 0.5 nm) by using thermally activated Fe nanoparticles [**289**]. In this technique, 15 nm diameter Fe nanoparticles diffuse into the few layer graphene at temperatures of ~ 900^{o}C and the Fe nanoparticles etched the graphene, as illustrated in Fig. 32 [**290**]. Inspection of the etch tracks reveals that they were spaced at 30^{o} intervals and the length and orientation of the etch tracks was correlated to that of the graphene lattice. Unlike conventional nanolithography techniques which have no selectivity toward the crystallographic orientation of the graphene lattice, the thermally activated Fe etching technique appears to be promising for constructing device edges that are oriented for circuit-level applications.

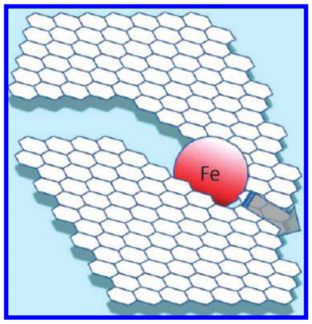

Figure 32. A schematic of the etching process in graphene or FLG using thermally activated Fe nanoparticles. With this technique the Fe nanoparticles etch graphene along crystallographic orientations which is useful to maintain the integrity of the edges for electronic device applications. Reprinted with permission from Reference [**290**]. Copyright 2008 American Chemical Society.

3.4 Transistor Applications of Graphene-Nanoribbons

The first GNR-FETS utilized e-beam lithography where oxygen plasma etching was used to pattern the monolayer thick graphene into ribbon widths between 15 – 100 nm [**25**]. The conductance of the GNRs was modulated by a gate voltage which varied by an one order of magnitude at room temperature, with transistor ON/OFF ratios of ~ 10^4 measured at 4 K . The energy gap for the narrowest ribbons with W ~ 15 nm were found to be ~ 200 meV [**287**]. While a dependence on the width was observed, no correlation was seen between the energy gap and etching the ribbon along different directions of the original graphene sheet; this has been attributed to the possibility of defects at the edges induced by the etching process.

GNR-FETs based on sub 10 nm wide and 10-60 nm GNRs have also been explored; the sub 10 nm GNRs were all found to be semiconducting and comprised of smooth edges which were obtained using a chemical synthesis approach [**287**]. FET-like devices were fabricated with GNRS having widths W ~ 10 nm – 55 nm. The channel length was 200 nm, and Pd was used as the source-drain contact, where the GNRs were back-gated with a 300 nm SiO_2 as the gate dielectric. From the measurements, the energy gap was calculated to be as high as ~ 400 meV.

Further examination of electrical performance was conducted on sub-10 nm GNR-FETs with Pd metal to form ohmic contacts for holes in the p-type transistors where the SiO_2 gate dielectric was 10 nm thick [**288**]. The 10 nm thick SiO_2 gate dielectric yielded better performance compared to the 300 nm SiO_2 used in previous work [**287**]. The performance of the GNR-FETs was also compared to CNT-FETS with Pd contacts and a 10 nm SiO_2, which yielded ON/OFF ratios as high as 10^6. The performance of the GNR-FETS was comparable to small diameter CNT-FETs with Pd contacts, but from a practical standpoint the GNR-FETS have advantages due to their all-semiconducting character. The general prospects for graphene-based electronic devices and systems appear to be exceptional, since in principle a wide variety of functionalities could be derived from a single sheet of graphene, ranging from conducting channels, quantum dots, interconnects, as well as transistors.

4.0 Suspended 1D Carbon Nanostructures for Nano-electro-mechanical-systems (NEMS) and Sensing

4.1 Introduction

In order to overcome the performance limiting issues in highly miniaturized Si transistors, an area of intense research is the use of nano-electro-mechanical-systems (NEMS) for microprocessor applications that are now gaining increasing attention, as indicated by the International Technology Roadmap for Semiconductors (ITRS) [**1**]. The physical isolation of conducting paths in NEMS reduces leakage currents and power dissipation, which are difficult to constrain with increasingly miniaturized Si transistors with short source-drain channel lengths or ultra-thin gate oxides. In addition, Si reverts to intrinsic behavior at low- and high-temperatures due to Fermi level shifting, which makes solid-state transistors more susceptible to thermal extremes. The underlying mechanical operation of NEMS structures is also suggestive of their inherent tolerance toward harsh thermal, as well as high radiation environments, which potentially enhances their ruggedness over solid-state transistors.

In particular, 1D carbon-based nanomaterials such as CNTs and CNFs offer advantages of exceptional elasticity for extending the mechanical cycling longevity of NEMS compared to inorganic nanowires, for example [**291**]. The success of CNT based NEMS has already been validated in a variety of applications ranging from nanotweezers [**292**], memory devices [**17**], nanorelays [**293**], [**19**], [**294**] and resonators [**295**]. In this chapter we will described the application of 1D CNTs and CNFs for NEMS applications. Since NEMS structures have to be isolated from the substrate as they represent moving parts, we will describe the methods used to suspend tubes in Section 4.2. In Section 4.3, mechanical switches based on single tubes will be discussed which are based on laterally (for planar 2D electronics), as well as vertically oriented tubes, which are potentially for 3D electronics. Then in Section 4.4, we provide a general overview of the use of arrays of SWNTs that are patterned using top-down lithography techniques to form NEMS architectures. The application of CNTs for NEMS mechanical resonators is then discussed in Section 4.5, with a particular emphasis on mass detection (arrays of NEMS resonators can also be potentially useful for filters in communications systems). Finally, in Section 4.6 we provide an example of an application of suspended tubes for physical sensing, specifically pressure sensing.

4.2 Approaches for Physically Suspending Tubes

The two primary approaches for forming suspended CNT structures are: a) post-growth release [**296**] or where the tubes are grown across pre-fabricated trenches on a wafer using thermal CVD [**297**], [**298**]. In both approaches, the AFM tip was used to mechanically strain the suspended tube(s) in order to understand how structural deformation affects the elastic strain in SWNT ropes [**298**] and the electronic transport properties of individual SWNTs [**298**]. At the Jet Propulsion Laboratory (JPL), both approaches have been implemented to form suspended CNT structures, but such structures have been exclusively used for device applications, specifically for NEMS actuators and pressure sensors described in more detail in Section 4.3 and 4.6, respectively.

4.2.1 Post Growth Release

Post-growth release was utilized at JPL with critical point drying to form suspended SWNTs that were used for pressure sensing [**299**], [**300**]. The operational mechanism of such sensors will be illustrated in Section 4.6. For the post-growth release approach, the SiO_2 beneath the SWNTs was etched in 10:1 Buffered-HF (BHF), which was followed by critical point drying. Simple drying techniques have been employed after HF etching to release < 1 μm long tubes by using the reduced surface tension of IPA (21.7 mN/m) [**301**], compared to that of DI water (72.8 mN/m), whereas the even lower surface tension of tetramethylsilane (10.2 mN/m) has also been utilized in other reports [**298**]. For the long SWNTs used in the JPL pressure sensor devices (5 – 10 μm), which are more susceptible to surface tension stress upon wet-release, added precautions were taken that employed critical point drying. The procedure for releasing the long tubes is described in more detail [**300**]. The electrical yield after release -- defined by the number of electrically conducting devices -- was > 90%, but the resistance was always higher after release. The rise in resistance could be associated with the contacts where the tubes are likely to exhibit kinks that suppress conductance.

4.2.2 Growth Across Pre-fabricated Trenches

The second technique used at JPL to suspend tubes relies on SWNTs to bridge the air-gap in prefabricated trenches. Such structures were utilized for lateral NEMS actuators that will be discussed in Section 4.3. In earlier reports, tubes were grown across prefabricated trenches, where the suspended tubes were over SiO_2/Si [**298**] substrates. In contrast, SWNTs were suspended over refractory Nb electrodes, for their application in NEMS switches, where the Nb served as the pull-electrode to electrostatically charge SWNTs in order to induce electromechanical switching. In general, the choice of the approach used to suspend tubes depends in part on the aspect ratio of the trenches, and on the quality of the tubes desired. For example, tubes that do not undergo post-growth processing are likely to be less defective, but such a technique is usually not feasible for forming suspended structures for low-aspect-ratio trenches below ~ 1:10; if the aspect ratio of the trench is too small, the tubes are likely to be undesirably draped on the substrate within the trench. This arises from the large amplitude vibrations that are thermally induced in the tubes from the high temperature CVD growth dynamics, increasing the likelihood of tubes attaching to the underlying substrate if the aspect ratio is too small.

4.3 Nano-Electro-Mechanical Switches Based on Single Carbon Nanotubes

For NEMS applications suspended or free-standing CNTs are necessary for them to serve as active actuating elements. NEMS-based actuators can serve as switches which exhibit reduced leakage currents and power dissipation, when compared to Si transistors where performance degrades with continued miniaturization. Due to the capacitive nature of switching in solid-state transistors, such devices are also susceptible to radiation and extremes in temperature, which is typically not the case with NEMS switches with their inherently mechanical construct. In section 4.3.1, NEMS switches that are based on tubes oriented laterally in a 2D planar configuration will be discussed, while in section 4.3.2, NEMS switches that are oriented perpendicular to the substrate are described.

4.3.1 *Two-Dimensional (2D) Planar NEMS Switches*

Electromechanical switching in CNTs was first observed by Rueckes *et al.* [**17**] where SWNTs were mechanically manipulated to form crossed structures with an air-gap. Switching has been demonstrated in deposited MWNT structures, where individual tubes were located by SEM for subsequent e-beam and thin film processing [**302**]. To date, switching in both SWNTs and MWNTs has been reported for the case of deposited tubes. An overview of the work conducted at JPL is provided here in developing SWNT NEMS switches [**19**], where the tubes are grown on-chip with patterned catalysts using materials that are compatible with the high temperature CVD synthesis of SWNTs. As described in Section 4.2, besides post-growth release [**296**], CNTs have also been grown across pre-fabricated trenches [**297**], [**298**] on a Si wafer, but in the JPL NEMS switches, the SWNTs are suspended over a refractory metal electrode made from Nb, which serves as the pull electrode to transiently charge the tube in order to induce electrostatic switching. A schematic of the architecture is shown in Fig. 33a and the details of the fabrication process are described in [**19**]. Shown in Fig. 33b is a high magnification SEM image of a SWNT crossing a 130 nm wide trench.

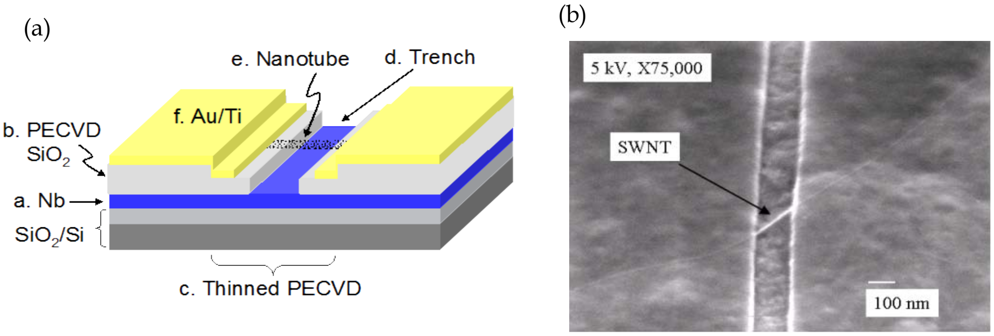

Figure 33. a) Schematic shows a nanotube switch composed of (a) a 200 nm Nb film deposited using DC magnetron sputtering onto a thermally oxidized Si wafer followed by (b) a 200 nm PECVD SiO_2 layer. (c) Active device regions are etched in the PECVD SiO_2 layer to a thickness of ~ 20 nm, the height of the air gap for the switch. (d) Nanotrenches are defined using e-beam and etched to the Nb layer. (e) SWNT are grown from patterned Fe in a CVD furnace using CH_4/H_2 (1500 sccm/50 sccm) at 850 °C. (f) Electrodes are deposited using e-beam evaporated Au/Ti (220 nm/12 nm) which are patterned using a bilayer resist/PMMA process for easy lift-off. b) High magnification SEM micrograph showing a single nanotube bridging the 130 nm wide trench. From Reference [**19**]. Copyright 2006 American Chemical Society.

The conductance between the left and right electrodes was measured and is shown in Fig. 34a, which yields a resistance of ~ 200 kΩ, much of which can be attributed to the high contact resistance between the CNT and the Au/Ti electrodes. In general, these resistances typically ranged in value from tens of kΩ to tens of MΩ's, where the presence of multiple tubes can also contribute to the differences in resistance. The actuation voltages were measured by applying a DC voltage between either the left or right electrode and the Nb pull electrode beneath the tube. As transient charge develops on the tube with increasing bias voltage, the resulting electrostatic force is sufficient to overcome the elastostatic force and deflects the suspended tube down toward the pull electrode.

Shown in Fig. 34b is an I-V characteristic of a device that was actuated over several cycles. In this case, turn-on occurs at ~ 2.4 V, and showed a variation with cycling that has also been reported in other CNT [**303**] and MEMS switches. The rapidly rising current regime arises in both the forward-biased (pull electrode grounded) and reverse-biased (pull electrode positive) cases, as indicated by the inset of Fig. 34b, although the exact switching voltages are slightly different in the two cases, ~ 2.4 V (forward-biased) and ~ 2.2 V (reverse-biased). The differences in turn-on voltage can perhaps arise from the random distribution of metallic and semiconducting tubes observed in current SWNT growth processes, but still suggests that the differences in resistance between the ON and OFF states far outweigh any differences that may arise from contact resistances. As shown by the inset of Fig. 34b, this switching behavior is polarity independent, as would be expected for electrostatic actuation, and rules out field emission as a likely mechanism at these voltages. In general, the magnitude of the switching voltages in these air-bridge devices is a few volts where the results were compared to first-order model calculations; the switching times were also determined to be small, on the order of a few nanoseconds [**19**], making them attractive for low power, high-frequency electronics applications.

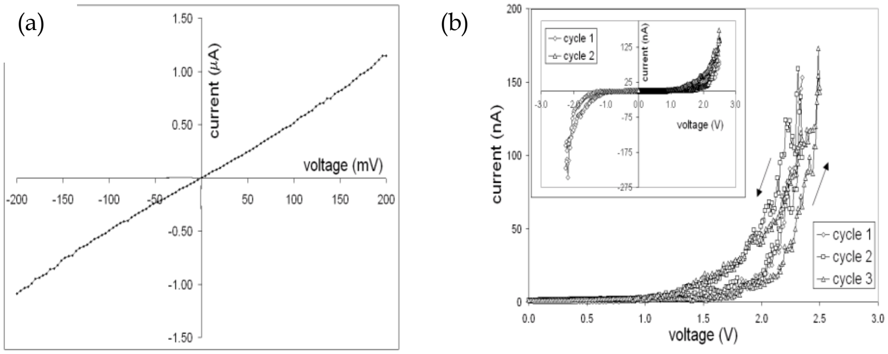

Figure 34. a) Conduction measurements from the left Au/Ti electrode to the right electrode for a typical device gives R ~ 200 kΩ (trench width ~ 250 nm, 2 μm x 5 μm catalyst area). b) I-V characteristic of a device actuated over multiple cycles (250 nm trench width). The inset shows the ON state voltage to be similar in the forward-bias (pull electrode grounded) and reverse-bias (pull electrode positive) regimes, indicating that field emission is an unlikely possibility at these voltages. From Reference [**19**]. Copyright 2006 American Chemical Society.

4.3.2 Three-Dimensional (3D) Vertical NEMS Switches

While the NEMS switches described in Section 4.3.1 were based on a 2D planar architecture, in this section we focus on a 3D NEMS architecture where the tubes are oriented vertically on a substrate, which has the potential to increase integration densities even further compared to 2D planar technologies. The vertical orientation of the tubes was made possible by the use of a plasma process, where Ni was used as the catalyst layer [**87**]. By lithographically patterning the Ni catalyst sites, it is possible to produce a single, vertically aligned tube or CNF at a pre-defined location using dc PECVD, as described in [**87**]. Electrostatic switching between vertically oriented tubes arranged in a 3-terminal configuration has been recently reported [**18**], [**304**]. In work conducted at JPL and the Kavli Nanoscience Institute (KNI) at Caltech, a nanoprobe inside an SEM was mechanically manipulated in order to electrically characterize single, vertically oriented CNFs to determine the suitability of such bottom-up synthesized structures for 3D NEMS applications [**305**]. Nanomanipulation was also used to interrogate individual, as-grown CNFs grown on Si, as well as those synthesized on refractory nitride under layers. The tubes were grown directly on Si <100> substrates with resistivity ρ ~ 1–5 m Ω-cm, and NbTiN. The ~ 200 nm thick refractory NbTiN was sputtered, with ρ ~ 113 μΩ-cm, and was also chemically compatible with CNF synthesis. The sample was mounted on a 45^{o} beveled holder inside the SEM, where tungsten probes on a nanomanipulator stage were used to make *in situ* electrical measurements with an HP 4155C parameter analyzer.

The nanoprobe was mechanically manipulated so that it physically contacted an individual CNF grown on NbTiN, where the ground probe was on substrate. Since the probe-to-tube contact length was < 100 nm for this 2-terminal measurement, conduction was dominated by the large contact resistance. The work function φ for tungsten (W) $\varphi_{W} \sim 4.5$ eV < $\varphi_{CNF} \sim 5.0$ eV [**306**], and suggests a Schottky barrier may arise at this interface, and also possibly at the tube-to-substrate interface; $\varphi_{NbN} \sim 3.92$ eV and like most transition metal nitrides with low φ [**307**], it is likely $\varphi_{NbTiN} < \varphi_{CNF}$. The role of the electrical contact to the substrate is important for the application of vertically oriented CNFs in NEMS and is discussed in more detail in [**305**].

Actuation measurements were performed for vertically oriented CNFs grown on NbTiN, where a nanoprobe was manipulated to within a few hundred nm of a single CNF. The electrostatic force per unit length F_{Elec} increases as $F_{Elec} \prec V^{2}$, where V is the voltage, and the elastostatic force per unit length F_{Elasto} increases as $F_{Elasto} \prec EI$, where E and I are the elastic modulus and moment of inertia of the nanotube, respectively [**308**]. With increasing V ($F_{Elec} > F_{Elasto}$) the tube deflects closer to the probe, and a tunneling current is detected which increases exponentially, and results in a sudden or sharp change in slope at turn-on. The switching I-V in Fig. 35 shows currents rising sharply at the pull-in voltage V_{pi} where $V_{pi} \sim 18$ V. The turn-off occurred at ~ 16 V and was dominated by the large tube-to-probe contact resistance since the tube remained stuck to the probe. The inset in Fig. 35 captures another switching event for a different tube, where turn-on and turn-off occurred at ~ 14 V and 10 V, respectively, and also illustrates the abruptness of the turn-on transition.

In many instances, stiction was seen in the CNFs after actuation, and suggests that the van der Waals force $F_{vdw} > F_{Elasto}$ which is validated by the hysteresis in the I-Vs of Fig. 35 and from other data reported in [**305**]. In earlier work [**304**], stiction was also reported for vertically oriented CNFs, but no hysteresis data was presented that electrically signaled the presence of stiction. Nonetheless, due to the apparently strong influence of van der Waals forces at these length scales, such structures appear to show promise for nonvolatile memory applications. These nanomanipulation measurements conducted also revealed that the CNFs synthesized directly on Si were not electrically conducting. Thus, such measurements suggest that the conducting nitride buffer layer (NbTiN) resulted in tubes that were electrically conducting via the sidewalls and thus suitable for low voltage 3D dc NEMS applications.

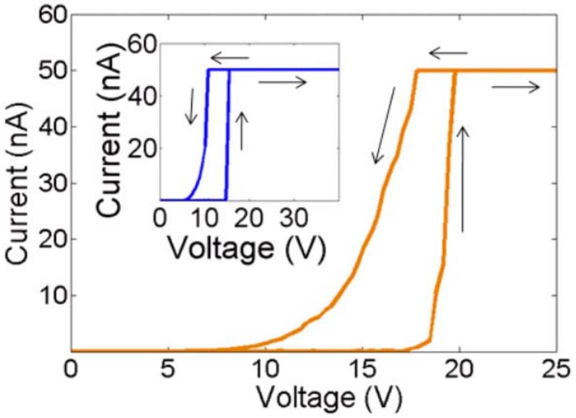

Figure 35. Actuation test where a nanoprobe was within hundred's of nm of a CNF. Turn-on and turn-off were at ~ 18 V and 16 V, respectively, where turn-off was dominated by the tube-to-probe contact resistance. The inset shows another tube where turn-on and turn-off occurred at ~14 V and 10 V, respectively, and also indicates the abruptness of the turn-on transition. From Reference [**305**]. Copyright 2009, American Institute of Physics.

4.4 Nano-electro-mechanical Switches Composed of Tube Arrays

While Section 4.3 was focused on the electrostatic switching in NEMS devices comprising of individual SWNTs, MWNTs, or CNFs, but monolayer thick fabrics comprised of arrays of CNTs are also being investigated and are a cornerstone of Nantero's mechanical memories [**309**]. In this application, monolayer thick fabrics of CNTs are formed by dispersing a prepared solution of SWNTs in a solvent onto a substrate and evaporating the solvent. The resulting 1-2 nm thick film is then patterned using conventional lithography and monolithically integrated with other CMOS processes to form laterally suspended monolayer thick fabrics that can be switched electrostatically for making non-volatile memory elements [**309**] for replacing Static-Random-Access-Memory (SRAM), Dynamic-Random-Access-Memory (DRAM) and Flash memory, for the defense, space, and commercial markets. Applications targeted are the formation of military and space-rated radiation-hard CMOS-CNT hybrid devices and circuits, and non-volatile memory products for the commercial marketplace. Monolayer thick fabrics composed of "SWNT wafers" over diameters as large as 6-inches have also been used to demonstrate mechanical switches though at longer micron length scales [**310**].

4.5 Carbon Nanotube Mechanical Resonators

Tubes in the bridge-type structures such as that shown in Fig. 33a can also be driven into vibration or resonance by an external perturbation such as an incoming AC signal. Much like a guitar string, the vibration frequency of the tube or suspended beam is a sensitive function of its mass. The smaller the total mass, the more sensitive it will be to the external perturbation, and the higher is its resonance frequency. The addition of any adsorbed mass on the tube or beam will cause a shift in its resonance frequency that can be measured and implemented for mass sensing, which is a well-examined application of such suspended structures.

Since sensitivity increases as beam dimensions shrink, there has been a constant push to drive the device dimensions to smaller and smaller length scales. For example, Si MEMS beams that resonate at RF frequencies, were used to detect species as small as bacteria and viruses as they adsorbed on a micro machined beam and caused a shift in its resonance frequency [**311**]. More recently, lithographically fabricated NEMS beams with their even smaller masses, high-frequency operation, and high Q's, were successfully used for the detection of protein molecules and nanoparticles [**312**]. Theoretical calculations suggest that mass sensitivity below a single Dalton could be achieved by making NEMS beams even smaller; this approach may be used for weighing individual atoms and for performing mass spectrometry, for example in proteomics, using a large-scale array of such sensors.

Resonance phenomena has also been observed in SWNTs [**313**], [**314**] which offer even more advantages than top-down fabricated MEMS and NEMS structures due to the remarkably high Young's modulus and the light structure of SWNTs. Such suspended SWNTs have been shown to act as oscillators, where the resonance frequency was measured using an indirect mixing technique. More recently, resonance was also observed in metallic MWNTs by using a direct on-chip transmission measurement technique where an RF displacement current was detected as the tube was driven into resonance [**295**]. Suspended CNTs are attractive as mechanical resonators and have significant promise for mass sensing applications, and arrays of such structures could also be beneficial for filters in communication systems.

4.6 Suspended Tubes for Pressure Sensing

Here we present an example of the application of suspended CNTs for passive physical sensing, specifically to sense pressure. Recently, CNT pressure sensors have been reported which were based on the mechanism of piezoresistance [**315**], [**316**]. In these recently reported CNT pressure sensors [**316**], metallic SWNTs were placed on membranes of atomic-layer-deposited (ALD) alumina, and a pressure differential across the membrane caused it to bulge, inducing strain in the overlying SWNT. Strain-induced conductivity changes were detected in non-vacuum environments (760-900 Torr). Unlike the mechanism of piezoresistance, a CNT pressure sensor was developed at JPL that operates on the principle of thermal exchange between a voltage-biased CNT and the surrounding gas [**299**], [**300**]. A recent article by Kawano *et al.* [**317**] presents a similar sensing mechanism, which utilized MWNTs grown using a localized synthesis process [**318**]. The JPL pressure sensors utilized SWNTs that were thermally grown with conventional CVD. Typical thermal conductivity gauges, such as Pirani or thermocouple gauges are physically large (volume ~ 10 cm^3) prohibiting their integration with many vacuum-encased Si-based micro-cavity applications (vacuum microelectronics, MEMS such as gyroscopes and RF MEMS switches). As a result of their large thermal mass, they are inherently slow, and also operate at high powers and temperatures.

With the advent of MEMS technology, miniaturized, low power pressure sensors were developed, representing the first application of bulk Si-micromachining [**319**]. Many of these Si-based transducers operate on the piezoresistive or capacitive principle [**320**] and obtaining wide-dynamic range has been challenging, which is especially important in micro-cavity applications. Due to the small volumes in micro-cavities, out gassing can cause large pressure changes over short times, affecting device performance.

In contrast, SWNT-based thermal conductivity gauge (volume ~ 10^{-4} cm^3) has been shown to operate at low power (nW-μW) and low temperature, and exhibits a wide dynamic range (760 Torr-10^{-6} Torr). Due to the reduced dimensionality for thermal conduction and phonon relaxation in 1D materials, transport is strongly influenced by environmental factors. The high surface area of the 1-D SWNT, along with the high temperature coefficient of resistivity (TCR) of diffusively contacted 5-10 μm long tubes, greater pressure sensitivity is enabled compared to thin-film or bulk conductors. Moreover, when the CNT is suspended, heat dissipation via the substrate is minimized, increasing sensitivity at even lower pressures.

A schematic of the device is shown in Fig. 36a where the starting substrate was a thermally oxidized Si <100> wafer. Patterned CVD growth of SWNTs using Fe-catalyst was performed, which was followed by e-beam deposition of Au/Cr electrodes (250 nm/5 nm) patterned by liftoff. In order to release the devices, the SiO_2 beneath the SWNTs was etched in BOE which was followed by critical point drying, as described briefly in Section 4.2.1 and also in [**300**]. A low magnification SEM image of a completed device is shown in Fig. 36b, which also shows the wire-bonds for electrically contacting the devices. The high magnification SEM image in Fig. 36c indicates a SWNT traversing the electrodes, where typical tube lengths were 5 – 10 μm.

The operational mechanism of such a thermal conductivity-based pressure sensor are described briefly. When a current passes through a wire lying on a substrate it induces joule heating. This heat can dissipate via several mechanisms, including the substrate (E_s), radiation (E_r) or the gas (E_g) [**321**] as shown by Eqn. (1) below; the input power supplied to the bias element is represented by an energy E_t where,

$$E_t = E_s + E_r + E_g \tag{1}$$

The heat dissipated through the substrate is (Are the equations numbered correctly?)

$$E_s = (K\Delta TA)/L \tag{2}$$

where A is the area through which heat transfer occurs, K is the thermal conductivity of the SiO_2, ΔT is the temperature difference between the current carrying element and the substrate and L is the distance from the element to the substrate.

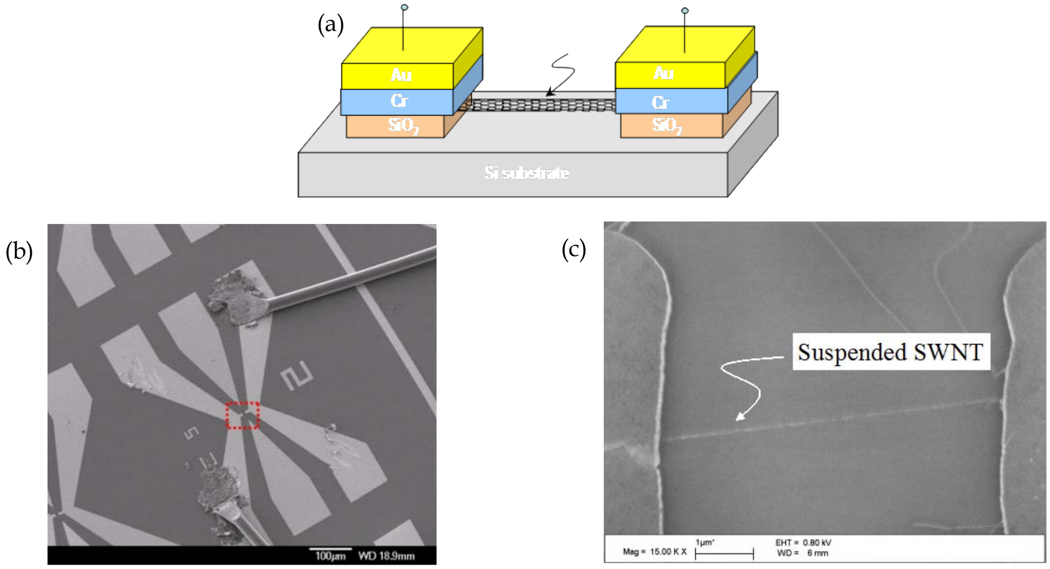

Figure 36. a) A schematic of the CNT pressure sensor where the SWNT is suspended. b) Low magnification SEM image of wire-bonded CNT vacuum gauge. Area highlighted by dashed lines indicates the region observed in the high magnification image in (c), where the typical SWNT lengths were 5-10 µm. Trench depth was ~ 310 nm. From Reference [**299**]. Copyright 2009 IEEE.

Radiative losses are given by (3) where σ is the Stefan-Boltzmann radiation constant, ε is the thermal emissivity of the element, and T_h and T_a are the temperatures of the element and ambient, respectively.

$$E_r = \sigma\varepsilon(T_h^4 - T_a^4)A \tag{3}$$

Finally, heat dissipation by the gas is given by E_g,

$$E_g = \alpha_r \Lambda_t AP(T_h - T_a)\sqrt{\frac{273}{T_h}} \tag{4}$$

where α_r is the accommodation coefficient, Λ_t is the free molecule thermal conductivity, A is the surface area of the element, and P is the pressure. While the radiative and substrate losses become more significant at low pressures, the thermal conductivity of the gas is a predominant loss mechanism in the viscous flow regime ($0.01 < K_n < 10$, where K_n is Knudsen's number). The heat dissipation in this regime depends linearly on pressure as illustrated by Knudsen's formula (Eqn. 4).

Shown in Fig. 37a, is the normalized current as a function of pressure for a thin-film meander resistor and a CNT device, both of which are biased at a few watts of power. The thin film resistor initially shows a conductance increase (up to about 200 Torr), a plateau region of constant current, and then current decreasing below about 20 Torr; the percent change in current is < 1%. In contrast, the CNT pressure sensor shows a rapid and continuous decrease in current from ambient to ~ 40 mTorr, with more than 35 % change in conductance.

At low pressures (< 100 mTorr), conduction through the gas becomes less significant and other pressure independent mechanisms such as radiative losses and solid-state conduction through the substrate tend to dominate, as seen by Eqns. 2 and 3. Radiative losses are significant only when temperatures exceed > 200 °C, and although radiative losses may be minimal at the low operational temperatures (or power) of our devices, the losses through the substrate have been calculated to be significant in the low vacuum regime. Post-growth release techniques, as described in Section 4.2.1, were used to remove the oxide beneath the tubes, and the pressure response of the suspended tubes was then measured.

Shown in Fig. 37b is the change in current which was measured as the pressure was reduced from ambient to vacuum for a device before and after it was released from the SiO_2 substrate. As it can be seen, the released CNT device has a continued decrease in conductance well into the 10^{-5} Torr range while the unreleased device shows little variation after about ~ 100 sec (~ 1 Torr), in this case. This data appears to confirm that by removing the substrate underneath the current carrying element, sensitivity is increased to the lower pressure ranges.

The increase in sensitivity after substrate removal is perhaps better exemplified by the data in Fig. 37c which shows the net current change (ΔI) for released and unreleased device in the pressure range of ~ 5 x 10^{-6} Torr to ~ 8 x 10^{-7} Torr. In both cases, ΔI increases with power but the released device has a three times larger change than that of the unreleased device (at a power of ~ 6 μW, $\Delta I_{released}$ ~ 550 nA, compared to $\Delta I_{unreleased}$ ~ 150 nA). The relationship of power effecting sensitivity appears to be in agreement with Fig.

37c, and the combined results suggest that the greatest sensitivity is expected for the released devices operated at high power.

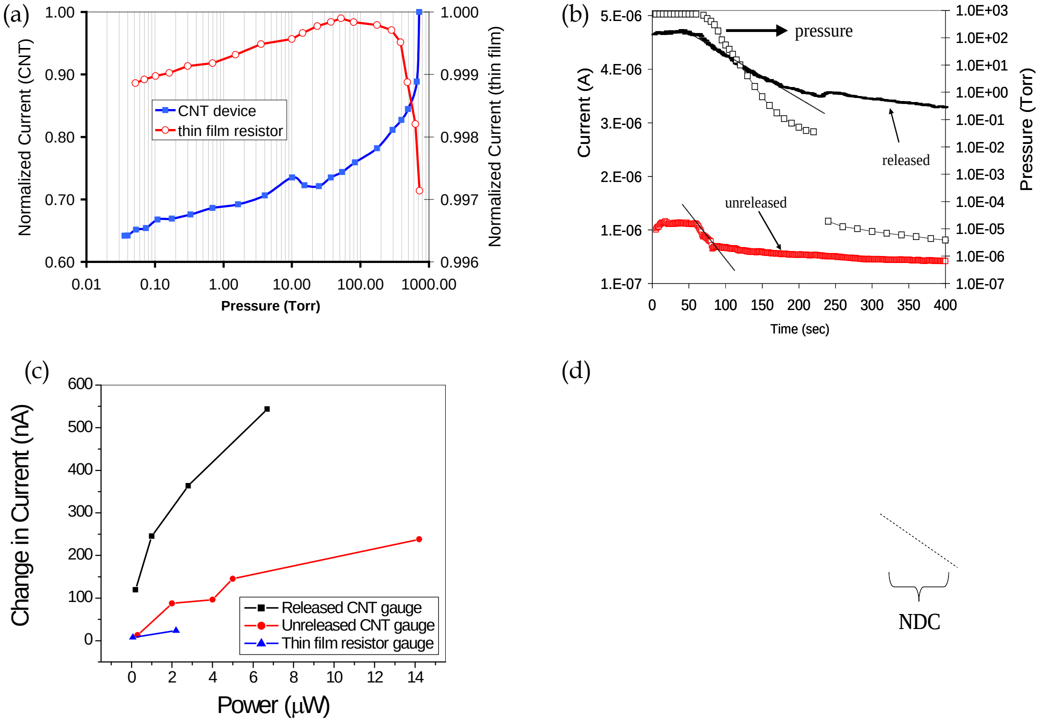

Figure 37. a) Normalized current-pressure response at 2 μW for thin film resistor and unreleased CNT device. The conductance change is smallest for thin film resistor (< 1 %) while the conductance continues to decrease for the CNT device by about 35% at 35 mTorr. b) Absolute current variation for released and unreleased device vs. time/pressure at ~2 μW. The released device shows a higher rate of conductance change down to ~10^{-6} Torr possibly due to minimizing heat loss through the substrate. c) Net current change from ~ 5 x 10^{-6} Torr to ~ 8 x 10^{-7} Torr for released and unreleased CNT sensors as a function of bias power. The thin film resistor gauge was the least sensitive. The largest change in conductance is for released device at high power levels. From Reference [**299**]. Copyright 2009 IEEE. d) The conductance of an unreleased SWNT device increases monotonically as the bias is increased, but after substrate removal, current saturation and a negative differential conductance (NDC) regime is observed in this device at high biases, which is attributed to the high optical phonon density in suspended tubes. Inset shows a higher current scale. From Reference [**300**]. Copyright 2009, IOP Publishing Limited.

While the increased current sensitivity with substrate removal can be explained on the basis of heat minimization through the substrate, the reduced dimensionality for phonon scattering in 1-D systems, in particular suspended SWNTs, can cause unique effects to arise at large bias voltages and power. At high fields, a large nonequilibrium optical phonon population exists in suspended SWNTs and their long relaxation times result in non-isothermal conditions along the length of the tube. The I-V characteristic of both suspended and unsuspended SWNTs has been iteratively calculated [**322**], by modeling the occupation probability of both optical and acoustic phonons at high biases, according to $I = \frac{V}{R(V,T)}$ where,

$$R(V,T) = R_c + \frac{h}{4e^2} \frac{\lfloor L + \lambda_{eff}(V,T) \rfloor}{\lambda_{eff}(V,T)} \tag{5}$$

Here, R_c is the contact resistance, L is the length of the nanotube and λ_{eff} is the sum of the acoustic, optical (emission) and optical (absorption) mean free paths derived from the Bose-Einstein phonon distribution. This analysis showed that in unsuspended tubes the I-V characteristic increases monotonically at high voltages since the substrate facilitates in the relaxation of optical phonons emitted through electron scattering, causing any heat to be dissipated via the substrate. In contrast, the current in the suspended tube saturates and a negative differential conductance (NDC) regime is encountered, which cannot be explained by velocity saturation (at ~ 5 kV/cm).

The NDC-regime has been observed in suspended SWNT devices at JPL, as shown by the I-V characteristic in Fig. 37d, where such measurements were taken in air and at room temperature. The unreleased device shows a monotonic rise in conductance, while the current after release for the same device saturates at high bias, ~ 2.8 V in this case, and enters a NDC regime. A peak conductance I_{peak}, where

$$I_{peak}(\mu A) = \frac{10}{L(\mu m)} \tag{6}$$

has been calculated and depends inversely on the length of the tube [**322**]. In the device shown in Fig. 37d, the experimentally observed I_{peak} was ~ 2.1 μA which appears to be in rough agreement with the expected value since the electrode spacing (and hence tube length) for this device was ~ 6 μm. Measurements show pressure sensitivity increases as the bias voltage or power are increased, but the released devices showed a more pronounced effect with power, as shown in Fig. 37c. At high fields, a large optical phonon density is observed, and with their longer lifetimes in suspended SWNTs, this may play an important role in determining the utility of such sensors for pressure or gas sensing. Finally, in order to improve robustness of the pressure sensors described here, it may be necessary to consider the use of tube bundles instead of single suspended tubes, which would enhance the reliability of such sensors for practical applications.

5.0 Silicon Nanowires (NWs) for Nanoelectronics and Nanophotonics

5.1 Introduction

Silicon has been the mainstay of the semiconductor industry and a harbinger of the microelectronics revolution and the thrust towards continuing miniaturization, via the ubiquitous Moore's law [**323**], has now extended to exploring the application of the element's nanostructures in various dimensionalities, such as thin films, nanowires, and quantum dots. In this paper, we briefly review the distinguishing electronic and lattice properties in one such manifestation of nanostructured silicon [**324**], i.e., Si nanowires (NWs). A major focus of this article is whether the NW form confers any special advantages, in addition to reduced size, to enable new fundamental physical insights and practical application. In this context, we will first consider the structure and assembly, through a study of fabricated ("top down") and synthesized ("bottom up") Si NW structures. The enhanced surface area to volume in NWs implies that the surfaces and interfaces play a more important role, than in the bulk, and will be considered. The reduced size is also important in altering the fundamental electronic band structure of Si, through quantum confinement effects, which will be explored next. Optoelectronic properties are closely associated to such issues. The implications of nanostructuring on the prevalent use of Si as a photovoltaic material will also be discussed. Subsequently, the properties of the lattice through an overview of the phononic properties will be done. The latter aspect is especially interesting in view of the recent proposal to use Si NWs as thermoelectric materials. It would be interesting, also, to consider and contrast Si NW structures with other well known one dimensional structures such as carbon nanotubes (CNTs) [**23**].

5.2 Synthesis of Silicon Nanowires (NWs)

Si NWs may be fabricated through both "top-down" approaches, i.e., through lithographic patterning or "bottom-up"/chemical synthesis of Si NWs. We will first consider a few methods for NW growth using the former approach and then review the use of CVD techniques, exploiting the VLS (Vapor-Liquid-Solid) and oxide-growth mechanisms. The section will then conclude with the outline of an approach to further reduce Si NW diameters.

5.2.1 Lithographic Patterning

Traditional lithographic methods, e.g., electron-beam lithography (EBL), can be used to fabricate Si NWs through the use of SOI (Silicon On Insulator) substrates, with a pre-determined Si thickness on top of SiO_2. The surface is then patterned with electron beam sensitive chemical resists and the oxide may then be removed through dry or wet etching. Through a careful control of process conditions, e.g., beam currents, reduced system noise, appropriate resist-developer combinations etc., NWs of diameters as small as 10 nm could be fabricated and practically used for field effect transistor (FET) and biosensing applications [**325**]. The lithographic method can be adapted to the controlled placement of both horizontal and vertically orientated NWs. Direct write EBL is capable of 10 nm resolution, and the throughput could be increased through wide area projection based EBL, such as the SCALPEL (SCattering with Angular Limitation in Projection Electron-beam Lithography) system developed by Bell labs [**326**] or the PREVAIL (Projection reduction Exposure with Variable Axis Immersion Lenses) technology of IBM [**327**].

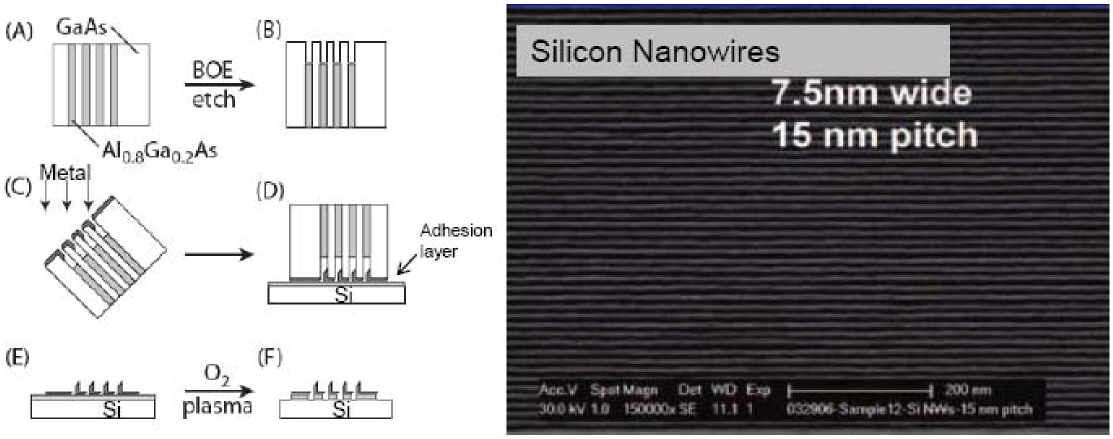

Figure 38. The SNAP method for fabricating Si NW arrays. (A) A GaAs/$Al_{0.8}Ga_{0.2}As$ superlattice fabricated by MBE is (B) preferentially etched to remove a part of the $Al_{0.8}Ga_{0.2}As$. (C) The etched substrate is used as a template for angled deposition of metal, e.g., Pt or Au, at the tips of the GaAs layers. (D) The substrate is then placed in contact with a Si wafer, with the aid of an adhesion layer and then (E) released though chemical etching. The metal lines remain on the wafer and serve as masks for etching Si NWs, say through reactive ion etching (RIE). The figure on the right shows a Si NW array made through this process. Figures adapted from [**336**] and [**338**].

Alternatives for the placement of arrays of Si NWs include the Nanoimprint Lithography (NIL) or the SNAP (Superlattice Nanowire Pattern Transfer) methods shown in Fig. 38 [**328**]. In the former, masks fabricated through EBL were used to imprint patterns into polymer films [**329**]. As an interesting variant of this scheme, in the SNAP method - superlattices, e.g., with alternating layers of GaAs and $Al_{0.8}Ga_{0.2}As$, fabricated through molecular beam epitaxy (MBE) were used as templates (Figure 1). The SNAP process can be used for NW fabrication from a native wafer of a given stoichiometry, doping, and crystallographic orientation. The width of the NWs can be controlled through the thicknesses of the superlattice layers and the NW length dictated by the substrate and can be of the order of mm [**330**]. Si NWs made through this process have been used for thermoelectric [**331**], arrays of field effect transistors (FETs) [**332**]and electronic devices with more complex architectures, such as cross-bar type electronic memories [**333**]. Alternately, chemical synthesis of Si NWs, using the "bottom-up" approach is being extensively used for wafer-scale growth, and *in situ* tunability of NW characteristics. We next outline two commonly used approaches using CVD based processes.

5.2.2 Vapor-liquid-solid (VLS) Mechanism

This method of Si NW growth is thought to proceed through the following sequential steps [**334**]: (1) adsorption of Si containing gaseous species on the surface of *molten* metal (e.g., Fe, Au, Ni) nanoparticle catalysts, (2) diffusion of Si through the catalyst, (3) nucleation and crystallization of Si at the liquid-solid interface, and (4) lateral nanowire growth. The diameters of Si NWs synthesized by invoking the VLS mechanism would be dictated by the size of the catalyst particle on the substrate while their length would depend on the duration of growth.

In one prototypical experiment, laser ablation of a $Si_{0.9}Fe_{0.1}$ solid target, at furnace temperatures around $1200^{o}C$ were shown [**335**] to yield ~ 6 nm - 20 nm diameter Si nanowires with lengths in the range of 1-30 μm. The high ambient temperature serves to maintain the ablated Si-Fe clusters in a molten state which then condense onto a cooler substrate. The supersaturation of the Si in the Fe was the driving force for the re-precipitation of the Silicon, when cooled, in the NW form as illustrated in Fig. 39. Consequently, the catalyst particle would often be found at one end of the NW.

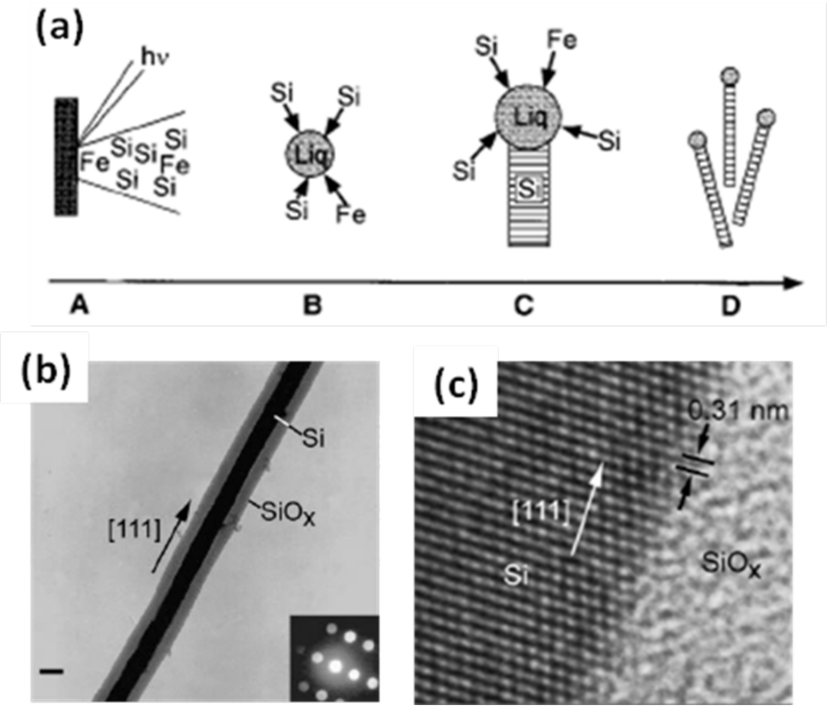

Figure 39. **(a)** A: Laser ablation of a $Si_{0.9}Fe_{0.1}$ target causes the formation of B: Si-Fe nanoclusters, which when cooled causes the C: precipitation of Si in the D: nanowire forms. Such a VLS (Vapor-Liquid-Solid) growth mechanism, with the characteristic formation of $FeSi_2$ particles at the ends is thought to be responsible for inducing NWs. The nanowires typically consist of a crystalline Si core surrounded by amorphous SiO_x as indicated by the **(b)** low resolution and **(c)** high resolution Transmission Electron Microscopy (TEM) micrographs. Figure adapted from [**343**].

In the VLS reaction sequence, it was observed that the growth rate was most dominated by the decomposition kinetics of the Si containing gaseous species, e.g. using Si_2H_6 as the gas source results in a 30 μm/minute growth rate while the use of silane (SiH_4) yields a growth rate of ~ 1 μm/minute. Such difference could presumably arise due to a larger chemical potential of Si in Si_2H_6 compared to SiH_4 *vis-a-vis* the chemical potential of Si in the NW. Typically, the metals for the catalyst particles are chosen for their ability to form low melting point eutectic alloys with Si e.g., ~ 640 K for Au-Si. The growth temperature could then, in principle, correspond to the eutectic temperature, e.g., 593 K [**336**]. However, this typically leads to defective NWs and consequently, higher growth temperatures (> 1000 K) along with a slow growth rate (< 10 μm/hour [**337**]) are used to reduce the number of defects. However, at such high temperatures larger catalyst particles form due to Ostwald ripening phenomena [**338**] and yield NWs > 10 nm in diameter. To bypass such thermodynamic size limitations, non-equilibrium techniques, such as laser ablation, have been attempted to produce smaller catalyst particles and have yielded smaller diameter (up to 3 nm) Si NWs [**335**], [**337**].

Additionally, the eutectic temperature may not correspond to that obtained from traditional phase diagrams, i.e., the liquidus temperature could also be significantly reduced, by as much as 100 K, due to enhanced interfacial energy contributions from smaller diameter catalyst particles [**339**]. The latter phenomena, e.g., the Gibbs-Thomson effect [**338**], would also reduce the amount of Si that can be incorporated in the catalyst particle and further limits the growth of smaller diameter NWs [**340**]. Typically, gas flow conditions and reaction temperatures can be adjusted for preferential growth of Si NWs in a particular direction, e.g., perpendicular to the substrate. For example, with growth on (100) Si substrates <111> oriented Si NWs would be expected to be dominant due to the lower surface energy of {111}, ~ 1.23 J/m^2 [**341**]. Experimentally [**342**], the following diameter distribution *vs.* orientation was noted for Si NWs: 3-10 nm - <110>, 10-20 nm - <112>, 20-30 nm - <111>. This result would imply that for smaller diameter NWs alternative, higher energy orientations, i.e., ~ 1.51 J/m^2 for <110> [**341**] are possible. Consequently, it can be surmised that the minimization of the sum of the interfacial and surface energies could dictate the NW orientation and not the latter alone.

The VLS mediated synthesis has also been postulated to be a relevant growth mechanism for a variety of other elemental and compound NW systems [**343**]. In the case of Si NWs, other experiments have implied the role of SiO_x present on the NWs, e.g., due to ambient oxygen, as integral to Si NW growth.

5.2.3 Oxide-assisted Growth

It was noted that the growth of Si NWs was greatly enhanced when SiO_2 containing Si powder targets were used in laser ablation, compared to (i) a metal containing target, e.g., $Si_{0.9}Fe_{0.1}$, (ii) a pure Si target, and (iii) a SiO_2 based target. It was then proposed that a thermally activated chemical reaction: Si (s) + SiO_2 (s)

→ 2 SiO (g), generates gaseous SiO species which decompose to Si nanoparticles and agglomerate to form Si NWs [**344**]. The Si nanoparticles embedded in an oxide matrix serve as nuclei for NW growth. Such a mechanism could explain the formation of linear as well as various nonlinear morphologies of NWs, e.g., spring-like (Fig. 40a), periodically interrupted (“fish-bone” type) or wires with a string of catalyst particles (“necklace” type)- (Fig. 40b), depending on whether single/multiple nucleation sites were involved and whether the growth occurred stably/unstably, respectively [**345**].

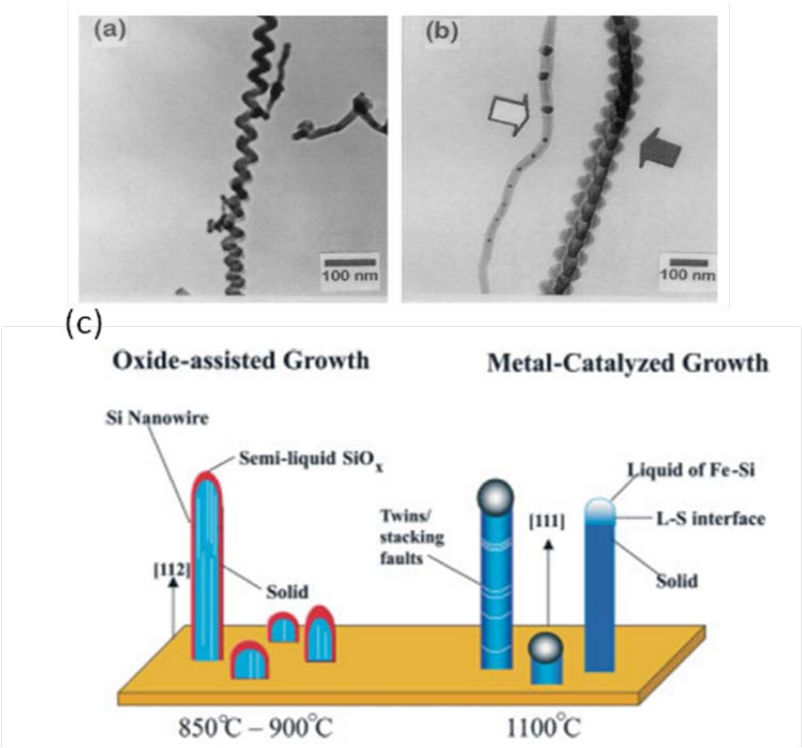

Figure 40. Alternative morphologies such as (a) spring-shaped and (b) fishbone structures can be obtained through invoking non-catalyst based oxide-assisted growth. (c) In comparison with the VLS method)Metal-catalyzed growth), in the oxide assisted growth method, lower temperatures of synthesis can be used leading to smaller diameter NWs with alternative orientations and greater morphological varieties. Figures adapted from [**352**] and [**353**].

It was also interesting to note that oxide assisted growth seemed to yield smaller diameter Si NWs (approaching 1 nm) and alternate crystalline orientations, i.e., <112> and <110> [**345**] Si NWs, formed through such a mechanism could be converted to the nanotube form, through thermally induced inner Si core melting [**346**] induced by exposure to intense radiation, (~ 0.2 J/m^2) i.e., a photographic flash.

5.2.4 *Self-limiting Oxidation for Reducing Si NW Diameters*

Si NWs, fabricated through lithographic patterning or chemical synthesis, can be further reduced in diameter through a self-limiting oxidation process [**347**]. For example, Si rods of diameters (~ 20 - 50 nm) fabricated through EBL [**347**] or (NIL) [**329**] based methods, were subject to dry oxidation at ~ 800-950 ^{o}C for various times (ranging from 0-15 hours). It was then seen that the oxide growth on the Si pillars undergoes a temperature dependent saturation [**348**] e.g., at ~ 24 nm at 850 ^{o}C and 16 hours (Fig. 41). Consequently, with an initial Si pillar diameter of ~ 30 nm, a 6 nm Si core can be obtained.

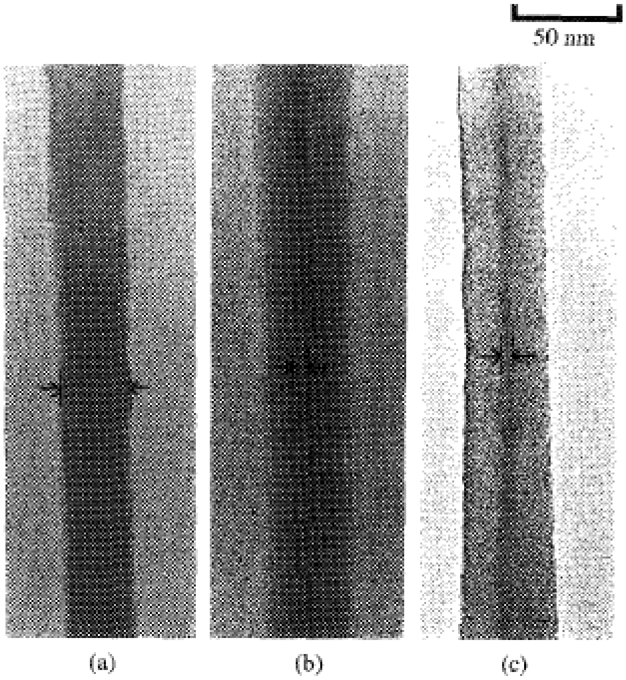

Figure 41. TEM micrographs of Si columns, fabricated through e-beam lithography and reactive ion etching (RIE), subject to increasing times of dry oxidation, i.e., (a) 0 h, (b) 8 h, and (c) 16 h at 850 ^{o}C. The initial (a) 30 nm diameter is gradually reduced to (b) 7 nm and (c) 6 nm. Figure adapted from [**79**].

Such a self-limiting oxide thickness is due to the stresses generated due to oxide growth at nonplanar Si/Si oxide interfaces [**349**] as are found in nanostructures [**350**]. Consequently, the initial oxide could be under tensile (/compressive) stress due to the convex (/concave) shape of the surface and promote thick (/thin) oxide layers [**351**]. In the case of oxide films on Si NWs the elastic energy increases with increasing thickness and at a certain value - the self-limiting thickness – is larger than the energy required for ambient oxygen to diffuse and oxidize the inner Si.

An alternative method to reduce Si NW diameter exploits electrochemical reactions [**352**], as are used for the synthesis of porous Si. In this case, fluoride ions in HF oxidize the Si and dissolve the surface layers. The extent of oxidation can be controlled through monitoring the current through the NW and tuned through the Si doping, concentration of electrolyte etc.

As with most other nanostructures, the controlled growth and placement of chemically synthesized Si NWs is quite challenging. While the CVD based methods provide vertically oriented NWs on a substrate there are obvious issues associated with electrically contacting the top surfaces. Consequently, various strategies have been used and are in development for directed and controlled growth [**353**] and/or assembly of Si NWs. This includes, for example, (a) *in situ* growth [**354**], (b) fluid assisted assembly [**355**], (c) alignment based on their polarizability [**79**] using localized electric fields (> 1 V/μm) [**356**] etc.

5.3 Influence of Interfaces and Defects

The enhanced influence of the surface area to volume ratio in Si NWs leads to an exaggerated importance for interfaces, defects, and issues such as surface reconstruction and passivation. As an example, from a consideration of the total energy of the NWs, including the surfaces and the facets in addition to the bulk energy, it was predicted that a *polycrystalline wire* with five-fold symmetry would have the lowest energy for NWs of diameter < 6 nm [**357**]. While such predictions imply that small diameter Si NWs could be intrinsically metastable, such morphology does not seem to have been experimentally observed to date.

Both from a thermodynamic and practical perspective, the presence of defects in Si NWs is inevitable and exerts a major influence on both electronic and lattice properties. For example, if Si NWs were to be used for transistors/switching devices [**358**] both extrinsic and intrinsic defects could influence the characteristics through effects such as a change in the threshold voltage [**359**], reduced carrier lifetime [**360**] etc.

However, defects do not seem to contribute to a reduction of the mechanical properties in NWs, e.g., elastic/bending modulus, compared to the bulk values. In fact, *in situ* atomic force microscopy (AFM) characterization has revealed [**361**] that theoretical cohesive strengths, close to 10% of the elastic modulus [**362**] could be approached in short length (< 600 nm) NWs. The influence of surface states has also been implicated in the 40-fold enhancement of the piezoresistance coefficient of Si NWs [**363**], compared to bulk values. The piezoresistance was shown to be increased through hydrogen passivation (using a HF treatment) and diminished with oxide formation (through HNO_3 mediated oxidation). While comprehensive explanations of these observations are still awaited the increased influence of strain and defects at such size scales are speculated.

Enhanced biochemical/molecular sensing seems to be feasible through the attachment of singular [**364**] atomic/molecular moieties to defects on Si NWs, as also observed for carbon nanotubes [**162**]. The underlying principle is the large surface area with an accompanying greater degree of change of electrical conductance - which is increased with decreasing NW diameter [**364**]. Additionally, electrochemical processes occur with a greater rate constant [**365**] enabling mass-transfer limited reactions with greater sensitivity compared to planar surfaces [**365**]. Defects also enable selective functionalization through a control of the type and amount of charge on the surface, e.g., through silanization of oxidized Si NWs [**366**] , using compounds such as APTES (Aminopropyltriethoxysilane) or OTS (Octadecyltrichlorosilane). Negative (/positive) surface charge can enhance(/reduce) the transit current in a *p*-type Si NW and can be used to tune electrical conductance and even cause a shift of the threshold voltage for current onset [**359**]. Additionally, the attachment of chemical moieties, e.g., ssDNA, to the functionalization agents and the consequent electrical current modulation also serves for sensing purposes [**366**]. Si NWs have also been shown to serve as templates for silica nanotubes [**367**] with relatively charge insensitive surfaces. Such nanoporous structures could be used for separation at the molecular level, through both size selectivity and electrochemical activity related to the aspect ratio, as evidenced through experiments on DNA translocation [**368**].

5.4 Electronic Properties

A fundamental modification of electronic properties from the bulk can be evidenced in Si NWs. For example, the indirect band gap (E_g ~ 1.1 eV) between the conduction band (CB) minimum and the valence band (VB) maximum, characteristic of bulk Si could be modified to a direct bandgap due to quantum confinement effects. In addition to such intrinsic effects, surfaces and defects also play a role, e.g., through exerting a greater influence on the valence band states (formed from *p*-orbitals) of the NWs, which are more localized compared to the conduction band states (formed from *s*-orbitals) [**369**].

5.4.1 Modification of The Energy Bandgap and Effects of Quantum Confinement

Motivated by the emission of light from Frenkel defect centers, i.e., C substitutional-Si interstitial pairs in bulk Si [**370**], the possibility of modification to the electronic E_g in lower dimensional Si structures was investigated [**371**]. It was then seen that, in Si monolayers terminated with H atoms, the electrical carrier confinement implies that a relatively constant energy would be needed for electron excitation, i.e., the *indirect* energy band gap would be similar to the *direct* E_g. A direct band gap is also made more feasible by the presence of electronegative atoms, e.g., O, F, Cl etc. which favor electron excitation in the absence of phonons, i.e., lower the direct bandgap energy relative to the indirect bandgap energy.

The enhanced coupling/interaction between the valence and the conduction band in lower dimensions, e.g., Si NWs has been interpreted in terms of zone-folding. This means that the CB minimum, normally situated along the <100> direction of the Brillouin zone (near the X-point) is folded back to be in proximity to the VB maximum at the center of the Brillouin zone (near the Γpoint) (Fig. 42) [**372**].

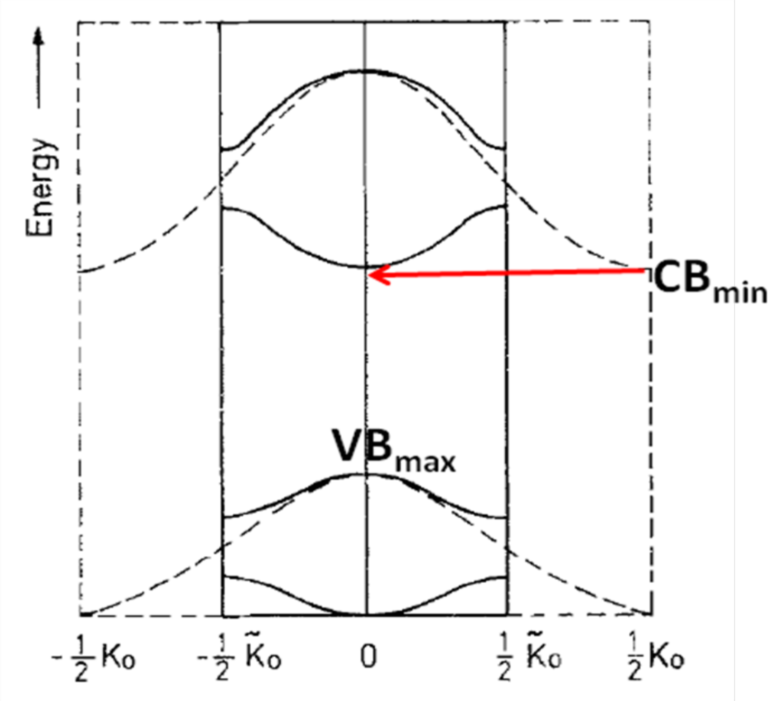

Figure 42. The band structure of bulk Si – *dotted line-* is modified - *solid line* – due to enhanced coupling between the valence and conduction bands in lower dimensions. The consequent zone folding, as represented by the movement of the conduction band minima (CB$_{min}$) to the zone center causes greater interaction with the valence band maxima (VB$_{max}$) yielding a band gap that is *quasi-direct.* Figure adapted from [**388**].

Molecular dynamics calculations have predicted that an indirect to direct energy band gap transition occurs in the 4.5-5.3 nm range for Si NWs oriented in the <111> direction [**373**], while smaller diameters (in the 1.4-2.1 nm range) are posited for <100> oriented NWs [**374**]. Now, the CB minima of bulk Si, at the X point, i.e., along <100>, has 6 equivalent valleys which are represented through anisotropic ellipsoids due to the different longitudinal (m_l= 0.19 m_e) and transverse (m_t= 0.92 m_e) masses. Consequently, the projections of the [100] oriented longitudinal and transverse valleys along the [100] NW axis are finite and the band gap remains indirect, while the [010] and [001] valleys project on the zone center, yielding a *direct* energy gap between the bands constituted from these valleys and the VB maxima.

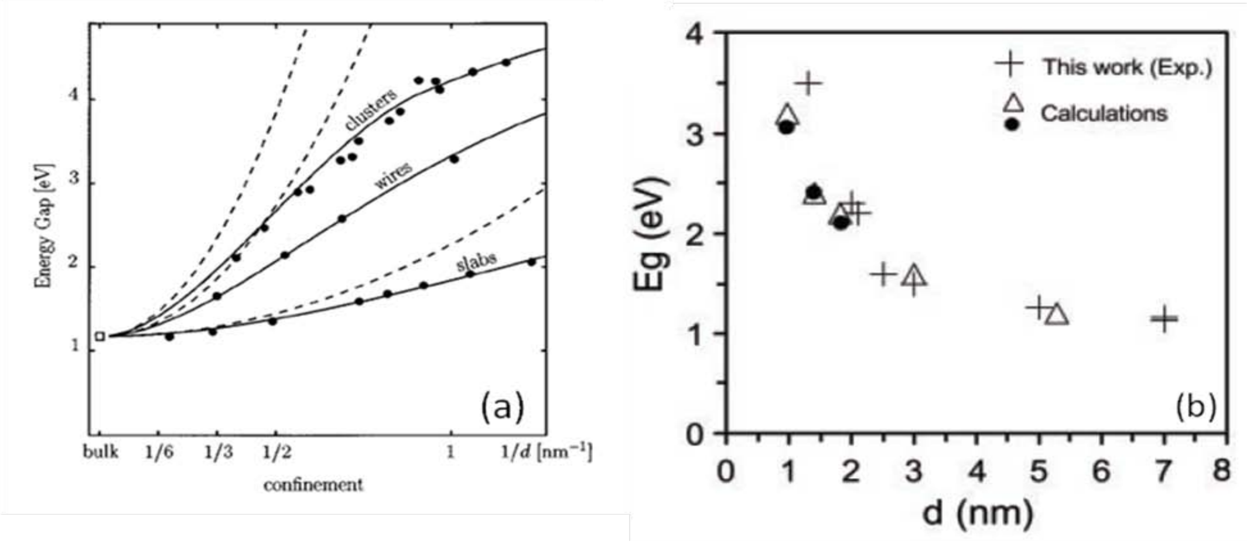

Figure 43. (a) The influence of quantum confinement in increasing the electronic energy gap (E_g) from the bulk value (~ 1.1 eV) obtained through DFT calculations. Figure taken from Reference [56] **(b)** Experimental measurements of the E_g variation with Si NW diameter as inferred through scanning tunneling spectroscopy (STS). Figures adapted from [**376**]. Calculations refer to the computational predictions from [**375**] (triangles)and [**377**] (dark circles).

The dependence of the energy gap on size and dimensionality has also been calculated [**375**] by density functional theory (DFT) in the local density approximation (LDA), with a self-energy correction of 0.6 eV, and shows a monotonic increase with decreasing length scale/ confinement parameter ($1/d$), as depicted in Fig. 43a. The experimental proof of such a bandgap increase was obtained through scanning tunneling spectroscopy (STS) measurements [**376**] on Si NWs with diameters in the 1.3 nm to 7 nm range, as illustrated in Fig. 43b [**377**]. The agreement between theory and experiment is remarkable.

5.4.2 Doping in Silicon Nanowires

Put There seems to be a general consensus through experimental observation that Si NWs are semiconducting at all sizes and can be doped [**378**] *n*-type or *p*-type, in a similar manner to bulk Silicon. Controlled doping, spanning a range of carrier concentrations, can be carried out through reactive gas flow (e.g. B_2H_6 for *p*-doping and P for *n*- doping Si [**378**] in CVD processes or through ion-implantation [**379**] [**380**]. Carrier depletion, due to the capture of electrons and holes by surface states and/or defects, is a major issue and results in a reduction from the expected value of the electrical carrier concentration. In very small diameter NWs (~ 3 nm), there is an additional tendency for dopants to segregate to the surface where they could combine with defects due to the lower formation energies associated with the surfaces [**381**] [62]. However, the difference in formation energies among surface and core substitutional sites is diminished for larger diameter NWs.

In the context of carrier depletion, it is commonly understood [**382**] that the Shockley-Reed-Hall (SRH) type recombination [**360**] mechanism which involves electrons/holes interacting with a localized state is dominant at low to moderate carrier concentrations. At higher carrier concentrations ($> 10^{17}$ /cm^3 – 10^{18} /cm^3) [**383**], Auger recombination would also play a role. The Auger mechanism involves the interaction of three carriers, e.g., the energy released by an electron and hole recombining is given to an electron or hole. However, an order of magnitude enhancement in the Auger recombination has been measured in hydrogen terminated Si (111) surfaces, even at carrier doping $\sim 3 \cdot 10^{15}$/cm^3 [**384**]. Such an increase suggests that when the extrinsic defect density, say contributing to SRH type recombination, is minimized alternative recombination mechanisms could become more important.

5.4.3 Electrical Conduction Mechanisms

If carrier depletion is present at the surface, electrical conduction takes place through the bulk of the NW by diffusion of electrical carriers and can be described through the Boltzmann formalism [**385**]. An experimental understanding of the electrical conduction mechanisms is often obtained through the placement of NWs as carrier channels in the MOSFET (Metal Oxide Semiconductor Field Effect Transistor [**386**]) configuration. In this case, the carriers (electrons/holes) move from a source to a drain through the NW channel whose conductivity is modulated by a metal gate separated from the channel by an insulating oxide. For channel lengths > 10 nm the effects of carrier tunneling between the source to drain can be ignored [**387**]. In studies on Si NW based MOSFETs [**358**] with channel lengths of the order of 50 nm and NW diameters around 10 nm [**388**] it was seen that classical electrostatics was adequate to explain the transistor characteristics.

A systematic variation of the active conduction length in undoped Si NWs was accomplished through the controlled fabrication of nickel silicide contacts, which could be diffused to different lengths along the NW through enhanced temperature annealing [**389**]. It was observed that for NW lengths < 1 μm the electrical transport was limited by the Schottky barriers at the metal-semiconductor interface while for lengths > 1 μm an *exponential* drop in the on-current (I_{on}) was seen. The latter could plausibly be due to the presence of defects and strain along the length of the NW. Consequently, in the shorter NWs the on-state current (I_{on}) was constant and a current modulation, i.e., I_{on}/I_{off}, of $\sim 10^7$ was seen. Such a dependence could be traced to the one-dimensional nature of carrier transport where defects/impurities can induce a strong resonant backscattering and reduce carrier mobility [**390**]. Coaxial structures where either the core or shell is doped can be effective in reducing carrier scattering effects. While discussing electrical conduction through Si NWs, it should be mentioned that their interfacing to external circuitry through Ohmic contacts is non-trivial [**391**]. In this context, the specific contact resistance (r_C) at a metal-Si interface was theoretically shown to have a lower limit of $\sim 10^{-9}\,\Omega\text{cm}^2$ [**392**]. Experimental observations have shown that for even optimally doped NWs the r_C values are two-three orders of magnitude higher [**393**]. This would imply for a 10 nm diameter Si NW, a contact resistance ($R_c = r_C/A$, where A is the contact area $= \frac{\pi}{4}(5\,nm)^2$) of the order of 5 kΩ and which increases with decreasing Si NW diameter. Additionally, as such low r_C values are obtained at high doping concentrations ($> 10^{20}/\text{cm}^3$), there is a greater scope for electrical carrier interactions which adversely affects the carrier mobility.

Alternatively, when quantum confinement effects are prevalent ballistic/non-diffusive transport can occur in the NWs. In the ballistic case, for example, the carrier mean free path is larger than the channel length. The motion of electrical carriers in the individual sub-bands or energy levels must be considered and the determination of the electrical conductance would involve the solution of the Schrodinger equation [**387**]. The quantization of electrical carrier energy leads to a discrete variation of the electrical conductance in units of $\frac{2e^2}{h}$ (~ 77 μS). Such effects have been seen in p-doped Ge core (10 nm diameter) /Si shell (2-5 nm) NWs, through a quantization of the energy levels in the Ge quantum well.

Finally, conduction through the surface states with energy levels in the bandgap provides an alternate channel for electrical transport. While simulations have shown [**373**] that the current-voltage (I-V) curves are unaffected by surface reconstruction, the possibility of edge state conduction mediated through surface states [**394**] [75] resulting in locally inhomogeneous current distribution has been posited.

5.5 Optical Properties

The possibilities of quantum confinement and a *direct* energy bandgap (Section 4.1) could modify the optical properties of Si NWs from those in the bulk. In this section, we will consider the characteristics relevant to NWs and their widely touted usage as solar cell materials.

5.5.1 Effects of Quantum Confinement in Small Diameter Nanowires

Generally, bulk Si is considered to be inefficient as a light emitter (or as a photodetector) due to the indirect energy bandgap, which means that electron-hole recombination for light emission is facilitated through lattice vibrations/phonons. The three particle requirement along with the lower electron-hole pair (exciton) coupling is the main impediment for enhanced efficiency. In the case of a direct energy bandgap, as can be obtained in Si NWs, larger optical coupling (two orders of magnitude greater than that of an indirect band gap) is possible between the VB maximum and the CB minimum and luminescence can be obtained. Additionally, with NW diameters below the exciton Bohr radius of ~ 4 nm for Si [**395**] quantum confinement effects would be expected to be more prominent.

The enhanced exciton coupling in direct bandgap Si NWs is also indicated through orders of magnitude increase in the exciton oscillator strength - a measure of the overlap of the electron and hole wave functions, which was shown to scale as 1/(NW diameter) [**374**]. Consequently, a 0.8 nm diameter Si NW was computed to have the same oscillator strength or luminescence efficiency of bulk GaAs. The exciton binding energies are also enhanced to > 0.1 eV in NWs and stable emission may be obtained at room temperature. In one experiment, peaks in the photoluminescence (PL) spectra were observed for 5 nm and 7.3 nm diameter Si NWs at around 1.8-2.0 eV while an additional peak at ~ 4.2 eV was seen for a 4.5 nm NW. While the former are more characteristic of indirect bandgap NWs [**396**], the peak at 4.2 eV is close to the expected value for the direct band gap at the Brillouin zone center [**377**] and indicates quantum confinement. The Si NWs, in this case, were synthesized in porous silica through a supercritical fluid (incorporating a mixture of diphenylsilane and CO_2) based technique. The intimate bonding of the NWs to the surrounding matrix was thought to reduce the effects of surface reconstruction and possible influence on the PL as often invoked in discussing emission from porous Si [**397**]. The possibility of PL due to transitions between strain induced (from the surrounding matrix) surface states was also proposed as a way to tailor the wavelength of the light emission. As excitonic effects are temperature dependent, PL intensity measurements along the length of the NW under a temperature gradient, as was done for GaN NWs [**398**], could be used to probe the characteristics of the surface states and their influence on the luminescence.

5.5.2 Optical Properties of Larger Diameter Silicon Nanowires for Photovoltaic Applications

In larger diameter (> 5 nm) NWs quantum effects are negligible and the optical properties can be understood through analogy with bulk Si properties. Such materials have been discussed with respect to their use in photovoltaic (PV) applications [**399**]which have been discussed in much detail elsewhere [**400**] [81]. We consider a few salient issues. Generally, the optimal direct E_g for solar energy conversion using PVs is ~ 1.4 eV [**401**]. However, Si with an indirect E_g of ~ 1.1 eV, in a *p-n* junction form is often preferred due to its relatively wide abundance, mature technology, and low cost [**400**]. Additionally, bulk Si has relatively low light absorption efficiency, with an absorption coefficient, α, at 550 nm – the peak of the solar spectrum of ~ 5830 cm^{-1} [**402**] in comparison to GaAs with an $\alpha \sim 6 \cdot 10^4$ cm^{-1}, due to its indirect bandgap. These α values imply that for 90% absorption approximately 100 μm thick Si would be needed [**403**]. Consequently, Si NWs which could exhibit absorption greater than a solid Si film [**404**] due to multiple reflection induced light trapping are relevant and have been studied for PVs. Another motivation was that NWs could allow for the use of relatively impure Si as it was proposed [**399**] that the large surface area concomitant with the small carrier diffusion length would improve light exposure and transduction to electrical power, respectively.

Generally, when a medium of refractive index, n (*e.g.,* n_{Si} ~ 4.077 + 0.028i at 550 nm) is in equilibrium with external black body radiation directly from the sun, there is an enhancement in intensity and absorption, in the medium, by a factor proportional to n^2. Such an increase is due to an increase in the density of states (DOS) which is proportional to k^2, where k ($=\frac{n\omega}{c}$) is the wave vector [**405**]. In the case of NWs, additional variables such as the geometry (length, diameter, pitch) would also need to be considered in determining the absorption. For example, the number of NW-photon interactions could decrease with increasing energy In contrast to absorption in a thin film. At low photon energies (sub-band gap) absorption from the surface states also needs to be taken into account. While regularly arranged/ordered Si NWs (> 50 nm diameter) have low reflectivity (<20%) over the 350 nm – 800 nm spectral range [**404**], [**406**] due to strong light trapping and scattering, it was noted [**407**] that disorder in the NWs could enhance the reflectivity - approaching 90% at λ = 800 nm.

Using principles common to bulk/thin film solar cells, attempts were made to fabricate p-n junctions in NWs to enable charge separation and power generation. This was most commonly done through (1) the assembly of n-doped NWs on p-type substrates [**408**], (2) vertical structures with p- and n-junctions on either ends of the wire [**409**] or axial p-i-n junctions [**410**]. However, the small junction area and exaggerated charge depletion effects (Section 3.1), both transverse and longitudinal to the NW, make such topologies unattractive [**411**]. Alternatively, arrays of radial p-n junction NWs, each with a core (*p*-type)-shell (*n*-type) structure [**412**]– Fig. 44 [**399**]was fabricated.

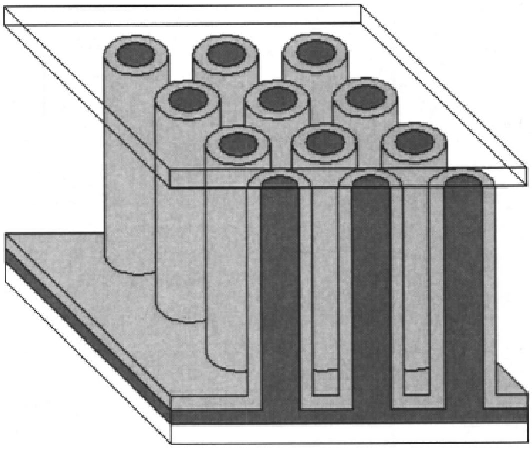

Figure 44. Schematic illustration of a radial p (*dark* gray) -n (*light* gray) junction based Si NW photovoltaics. Figure adapted from [**417**].

In the core-shell NW structures, it was determined that if the (a) the radius of the p-core is approximately equal to the minority carrier diffusion length, (b) the core and shell has a sufficiently high doping concentration to avoid depletion, and (c) there is low trap density in the depletion region ($< 10^{15}/cm^3$), then PV efficiency could be optimized. Combined with the requirement of achieving a low contact resistance the above conditions stipulate that Si NW diameters could be in the 100 nm – 2 μm [**413**] range. It was also interesting to note that the specific shape of the Si NW could be important [**413**], as garnered through measurements on a single 900 nm diameter hexagonal faceted Si NW, where the p-n junction was constituted of a n-type Si NW with the p-side facilitated through Al contacts.

The reported efficiencies of Si NW based solar cells are at the present quite low, ranging from 0.1%[**408**] to 3.4% [**412**] for p-i-n structures to 9.31% [**406**]. However, there seems to be scope for improvement through the use of heterojunction and hybrid structures [**402**] and methods to enhance light absorption [**414**]. For example, infiltrating voids between the NWs with higher index media, e.g., ethanol with an index of 1.36, was proposed to improve absorption through an increased light scattering mean free path [**415**]. Additionally, using a gradual change of refractive index from the top to the bottom of the NW array could minimize abrupt reflection [**416**], i.e., at normal incidence 98% of the incident light was found to be absorbed through the use of Si nanocone arrays (tapering from 20 nm at the top to 300 nm at the bottom) in comparison to the 85% light absorption for Si NW arrays and 78% absorption for thin films. It would also be interesting to consider whether recent results [**417**] in the enhancement of the refractive index, due to birefringence in anisotropic media can be applied to increase light trapping in Si nanowire media.

Silicon nanowires are a manifestation of the influence of nanoscience and technology on one of the most widely studied bulk material of the past few decades. In this paper, we have outlined salient features of these nanostructures with an emphasis on various methods of synthesis and their characteristic properties. The possibilities of miniaturization have been used to apply Si NWs for electronic devices, photovoltaics, battery electrode materials, thermoelectrics etc., with a goal of improved efficiency in performance and power consumption. Other aspects relevant to the size reduction such as giant piezoresistance in Si NWs [**363**] and their use as ultra-sensitive nano-electro-mechanical systems (NEMS) [**418**], [**419**] could be pertinent for high resolution and mass sensitivity applications. However, the aspect of semiconducting Si NWs that seems to be most interesting from the point of view of developing new scientific and technological paradigms involves the aspect of quantum confinement. It was seen that such paradigm development mandates Si NWs of sub 5 nm diameters, the controlled and large scale synthesis of which seems to be quite challenging at the present. Additionally, as with most nanotechnology which requires controlled placement of nanostructures the growth and arrangement of such small diameter NWs is quite challenging. It is then thought that studies focused on the science of Si NWs are crucial, prior to deciding whether the technological effort on large scale assembly is necessary.

6.0 ~~Conclusion and Future Directions~~Summary

In this review, we have provided an overview of the physical properties, synthesis techniques and the applications of 1D Carbon and Silicon nanostructures for electronics and photonics. While the ~~invention of the~~ Silicon transistor has enabled the microelectronics industry to progress exponentially over the past five decades according to Moore's Law, fundamental challenges lie in the road ahead toward continued miniaturization. In this chapter, we have discussed the use of low-dimensional~~ity~~ carbon and Si based nanomaterials for potentially overcoming such inherent challenges~~ posed by the traditional materials used in the Si IC industry~~.

The digital and analog applications of CNTs, along with their use as interconnects, ~~was discussed in Section 1.0. In Section 2.0,~~along with other novel manifestations, such as branched carbon nanostructures, ~~specifically~~ e.g., Y-~~y~~-junctions, ~~were discussed that~~may enable new device functionality in novel transistor architectures. The ~~first experimental~~ synthesis of graphene ~~in 2004 opened~~ also reveals~~up~~ new possibilities for the application of ~~low-dimensionality~~ carbon nanostructures such as GNRs, particularly for high-performance transistor applications~~; this discussion was presented in Section 3.0.~~ Some practical applications, such as m~~M~~echanical nanorelays are ~~also~~ gaining increasing attention both for dc switches and ac resonator applications, ~~which was highlighted in Section 4.0~~in view of the requirements for lower power consumption switching devices, with low switching currents. ~~Finally, in Section 5.0, we presented~~ R~~r~~ecent progress in the synthesis of ~~the use of low-dimensionality Si nanostructures, specifically~~ Si nanowires ~~for optical applications~~along with a chractareization of their electronic and photonic properties may open up new vistas in the continued of Silicon. While significant developmental efforts are still necessary in order to drive such nanomaterials from the lab and into the commercial market place, tremendous progress seems to have~~s~~ been achieved in ~~both~~ the sciencti‌fic aspects ~~e and the technological developments of these materials~~ over the past two decades.

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8.0 References

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[1] International Technology Roadmap for Semiconductors; http://www.itrs.net/reports.html, 2007 Edition.

[2] M. S. Dresselhaus, G. Dresselhaus, P. Avouris (Eds.), Carbon Nanotubes, Springer, Berlin, 2001.

[3] P. Avouris, Z. Chen, and V. Perebeinos, *Nat. Nanotechnol.* **2**, 605 (2007).

[4] Q. Cao and J. Rogers, *Adv. Mater* **21**, 29 (2009).

[5] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, *Science* **294**, 1317 (2001).

[6] Z. Zhang, X. Liang, S. Wang, K. Yao, Y. Hu, Y. Zhu, Q. Chen, W. Zhou, Y. Li, Y. Yao, J. Zhang, and L. M. Peng, *Nano Lett.* **7**, 3603 (2007).

[7] J. Appenzeller, Y. Lin, J. Knoch, Z. Chen, and P. Avouris, *IEEE Trans. Electron Devices* **52**, 2568 (2005).

[8] P.R. Bandaru, C. Daraio, S. Jin, and A.M. Rao, *Nature Materials* **4**, 663 (2005).

[9] J. Li, A. Cassell, H. T. Ng, R. Stevens, J. Han, and M. Meyyappan, *Appl. Phys. Lett.* **82**, 2491 (2003).

[10] H. Li, C. Xu, N. Srivastava, and K. Banerjee, *IEEE Trans. Elect. Dev.* **56**, 1799 (2009).

[11] W. B. Choi, D. S. Chung, J. H. Kang, H. Y. Kim, Y. W. Jin, I. T. Han, Y. H. Lee, J. E. Jung, N. S. Lee, G. S. Park, and J. M. Kim, *Appl. Phys. Lett.* **75**, 3129 (1999).

[12] F. Lu, L. Gu, M. J. Meziani, X. Wang, P. G. Luo, L. M. Veca, L. Cao, and Y. P. Sun, *Adv. Mater.* **21**, 139 (2009).

[13] C. Yu, S. Saha, J. Zhou, K. Shi, A. M. Cassel, B. A. Cruden, Q. Ngo, and J. Li, *J. Heat Transfer-Trans. ASME* **128**, 234 (2006).

[14] P. Wei, W. Bao, Y. Pu, C. N. Lau, and J. Shi, *Phys. Rev. Lett.* **102**, 166808 (2009).

[15] H. Ago, K. Petritsch, M. S. P. Shaffer, A. H. Windle, and R. H. Friend, *Adv. Mater.* **11**, 1281 (1999).

[16] Y. Homma, S. Chiashi, and Y. Kobayashi, *Reports on Progress in Physics* **72**, 066502 (2009).

[**17**] T. Rueckes, K. Kim, E. Joselevich, G. Y. Tseng, C. L. Cheung, and C. M. Lieber, *Science* **289**, 94 (2000).

[**18**] J. E. Jang, S. N. Cha, Y. J. Choi, D. J. Kang, T. P. Butler, D. G. Hasko, J. E. Jung, J. M. Kim, and G. A. J. Amaratunga, *Nat. Nanotech.* **3**, 26 (2008).

[**19**] A. B. Kaul, E. W. Wong, L. Epp, and B. D. Hunt, *Nano Lett.* **6**, 942 (2006).

[**20**] M. F. Yu, O. Lourie, M. J. Dyer, K. Moloni, T. F. Kelly, and R. S. Ruoff, *Science* **287**, 637 (2000).

[**21**] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, *Science* **306**, 666 (2004).

[**22**] H. W. Kroto, J. R. Heath, S. C. O'Brien, R. F. Curl, and R. E. Smalley, *Nature* **318**, 162 (1985).

[**23**] S. Iijima, *Nature* **354**, 56 (1991).

[**24**] S. Iijima and T. Ichihashi, *Nature* **363**, 603 (1993).

[**25**] M. Han, B. Ozyilmaz, Y. Zhang, and P. Kim, *Phys. Rev. Lett.* **98**, 206805 (2007).

[**26**] R. Saito, G. Dresselhaus, and S. Dresselhaus, *Physical Properties of Carbon Nanotubes*. London, U. K.: Imperial College Press, 1998.

[**27**] V. Crespi and M. Cohen, *Phys. Rev. Lett.* **75**, 2093 (1997).

[**28**] T. Odom, J. Huang, P. Kim, and C. M. Lieber, *Nature* **391**, 62 (1998).

[**29**] J. W. G. Wildoer, L. C. Venema, A. G. Rinzler, R. E. Smalley, and C. Dekker, *Nature* **391**, 59 (1997).

[**30**] M. S. Arnold, A. A. Green, J. F. Hulvat, S. I. Stupp, and M. C. Hersam, *Nat. Nanotechnol.* **1**, 60 (2006).

[**31**] T. W. Odom, J. L. Huang, P. Kim, and C. M. Lieber, *J. Phys. Chem.* **194**, 2794 (2000).

[**32**] S. Frank, P. Poncharal, Z. Wang, and W. A. de Heer, *Science* **280**, 1744 (1998).

[**33**] A. Bachtold, M. Fuhrer, S. Plyasunov, M. Forero, E. Anderson, A. Zettl, and P. McEuen, *Phys. Rev. Lett.* **84**, 6082 (2000).

[**34**] T. Durkop, S. A. Getty, E Cobas, and M. S. Fuhrer, *Nano Lett.* **4**, 35 (2004).

[**35**] Z. Yao, C. L. Kane, and C. Dekker, *Phys. Rev. Lett.* **84**, 2941 (2000).

[**36**] W. I. Milne, K. B. K. Teo, G. A. J. Amaratunga, P. Legagneux, L. Gangloff, J. P. Schnell, V. Semet, V. T. Binh, and O. Groening, *J. Mater. Chem.* **14**, 933 (2004).

[**37**] Y. C. Chen, N. R. Raravikar, L. S. Schadler, P. M. Ajayan, Y. P. Zhao, T. M. Lu, G. C. Wang, and X. C. Zhang, *Appl. Phys. Lett.* **81**, 975 (2002).

[**38**] J. A. Misewich, R. Martel, P. Avouris, J. C. Tsang, S. Heinze, and J. Tersoff, *Science* **300**, 783 (2003).

[**39**] M. Freitag, V. Perebeinos, J. Chen, A. Stein, J. Tsang, J. Misewich, R. Martel, and P. Avouris, *Nano Lett.* **4**, 1063 (2004).

[**40**] Z. Yang, L. Ci, J. A. Bur, S. Y. Lin, and P. M. Ajayan, *Nano Lett.* **8**, 446 (2008).

[**41**] K. Mizuno, J. Ishii, H. Kishida, Y. Hayamizu, S. Yasuda, D. N. Futaba, M. Yumura, and K. Hata, *Proc. Natl. Acad. of Sci. U.S.A.* **106**, 6044 (2009).

[**42**] J. P. Salvetat, J. M. Bonard, N. H. Thomson, A. J. Kulik, L. Forro, W. Benoit, and L. Zuppiroli, *Appl. Phys. A* **69**, 255 (1999).

[**43**] B. I. Yakobson and R. E. Smalley, *Am. Sci.* **85**, 324 (1997).

[**44**] M. Nardelli and J. Bernholc, *Phys. Rev. B* **60**, R16338 (1998).

[**45**] A. Rochefort, D. Salahub, and P. Avouris, *Chem. Phys. Lett.* **297**, 45 (1998).

[**46**] C. Park, Z. Ounaies, K. A. Watson, R. E. Crooks, J. Smith, S. E. Lowther, J. W. Connell, E. J. Siochi, J. S. Harrison, and T. L. S. Clair, *Chem. Phys. Lett.* **364**, 303 (2002).

[**47**] W. Zhou, J. Vavro, C. Guthy, K. I. Winey, J. E. Fischer, L. M. Ericson, S. Ramesh, R. Saini, V. A. Davis, C. Kittrell, M. Pasquali, R. H. Hauge, and R. E. Smalley, *J. Appl. Phys.* **95**, 649 (2004).

[**48**] Y. L. Li, I. A. Kinloch, and A. H. Windle, *Science* **304**, 276 (2004).

[**49**] C. Yu, L. Shi, Z. Yao, D. Li, and A. Majumdar, *Nano Lett.* **5**, 1842 (2005).

[**50**] J. Hone, M. Whitney, C. Piskoti, and A. Zettl, *Phys. Rev. B-Condens. Matter* **59**, R2514 (1999).

[**51**] C. Kittel, *Introduction to Solid State Physics*, 8th ed. New York: Wiley, 2004.

[**52**] H. Y. Chiu, V. V. Deshpande, H. W. Postma, N. Lau, C. Miko, L. Forro, and M. Bockrath, *Phys. Rev. Lett.* **95**, 226101 (2005).

[**53**] L. G. C. Rego and G. Kircezenow, *Phys. Rev. Lett.* **81**, 232 (1998).

[**54**] D. S. Bethune, C. H. Kiang, M. S. Devries, G. Gorman, R. Savoy, J. Vasquez, and R. Beyers, *Nature* **363**, 605 (1993).

[**55**] A. Thess, R. Lee, P. Nikolaev, H. Dai, P. Petit, J. Robert, C. H. Xu, Y. H. Lee, S. G. Kim, A. G. Rinzler, D. T. Colbert, G. E. Scuseria, D. Tomanek, J. E. Fischer, and R. E. Smalley, *Science* **273**, 483 (1996).

[**56**] N. Franklin and H. Dai, *Adv. Mater.* **12**, 890 (2000).

[**57**] A. Cassel, N. Franklin, T. Tombler, E. Chan, J. Han, and H. Dai, *J. Amer. Chem. Soc.* **121**, 7975 (1999).

[**58**] A. C. Dupuis, *Prog. Mater. Sci.* **50**, 929 (2005).

[**59**] G. Y. Zhang, D. Mann, L. Zhang, A. Javey, Y. M. Li, E. Yenilmez, Q. Wang, J. P. McVittie, Y. Nishi, J. Gibbons, and H. J. Dai, *Proc. Natl. Acad. Sci. U.S.A* **102**, 16141 (2005).

[60] Q. Cao, S. H. Hur, Z. T. Zhu, Y. Sun, C. Wang, M. A. Meitl, M. Shim, and J. A. Rogers, *Adv. Mater.* **18**, 304 (2006).

[61] Y. L. Li, L. H. Zhang, X. H. Zhong, and A. H. Windle, *Nanotech.* **18**, 225604 (2007).

[62] S. Maruyama, R. Kojima, Y. Miyauchi, S. Chiashi, and M. Kohno, *Chem. Phys. Lett.* **360**, 229 (2002).

[63] K. Hata, D. N. Futaba, K. Mizuno, T. Namai, M. Yumura, and S. Iijima, *Science* **306**, 1362 (2004).

[64] C. J. Lee, K. H. Son, J. Park, J. E. Yoo, Y. Huh, and J. Y. Lee, *Chem. Phys. Lett.* **338**, 113 (2001).

[65] G. D. Nessim, M. Seita, K. P. O'Brien, A. John Hart, R. K. Bonaparte, R. R. Mitchell, and C. V. Thompson, *Nano Lett.* **9**, 3398 (2009).

[66] M. Cantoro, S. Hofmann. S. Pisana, C. Ducati, A. Parvez, A. C. Ferrari, and J. Robertson, *Diamond Relat. Mater.* **15**, 1029 (2006).

[67] G. Takeda, L. Pan, S. Akita, and Y. Nakayama, *Jpn. J. Appl. Phys.* **44**, 5642 (2005).

[68] Y. Nakayama, L. Pan, and G. Takeda, *Jpn. J. Appl. Phys.* **45**, 369 (2006).

[69] S. Sato, A. Kawabata, D. Kondo, M. Nihei, and Y. Awano, *Chem. Phys. Lett.* **402**, 149 (2005).

[70] S. Sato, A. Kawabata, T. Nozue, D. Kondo, T. Murakami, T. Hyakushima, M. Nihei, and Y. Awano, *Sensors and Materials* **21**, 373 (2009).

[71] S. Hofmann, C. Ducati, J. Robertson, and B. Kleinsorge, *Appl. Phys. Lett.* **83**, 135 (2003).

[72] M. Chhowalla, K. B. K. Teo, C. Ducati, N. L. Rupensinghe, G. A. J. Amaratunga, A. C. Ferrari, D. Roy, J. Robertson, and W. I. J. Milne, *J. Appl. Phys.* **90**, 5308 (2001)

[73] G. F. Zhong, T. Iwasaki, K. Honda, Y. Furukawa, I. Ohdomari, and H. Kawarda, *Jpn. J. Appl. Phys. Part 1* **44**, 1558 (2005).

[74] G. H. Jeong, N. Satake, T. Kato, T. Hirata, R. Hatakeyama, and K. Tohji, *Appl Phys. A* **79**, 85 (2004).

[75] C. Bower, O. Zhou, W. Zhu, D. J. Werder, and S. Jin, *Appl. Phys. Lett.* **77**, 2767 (2000).

[76] D. H. Kim, H. S. Jang, C. D. Kim, D. S. Cho, H. S. Yang, H. D. Kang, B. K. Min, and H. R. Lee, *Nano Lett.* **3**, 863 (2003).

[77] R. E. Morjan, V. Maltsev, O. Nerushv, Y. Yao, L. K. L. Falk, and E. E. B. Campbell, *Chem. Phys. Lett.* **383**, 385 (2004).

[78] S. J. Kang, C. Kocabas, H. Kim, Q. Cao, M. A. Meitl, D. Khang, and J. A. Rogers, *Nano Lett.* **7**, 3343 (2007).

[79] E. Joselevich and C. M. Lieber, *Nano Lett.* **2**, 1137 (2002).

[80] Y. G. Zhang, A. L. Chang, J. Cao, Q. Wang, W. Kim, Y. M. Li, N. Morris, E. Yenilmez, J. Kong, and H. J. Dai, *Appl. Phys. Lett.* **79**, 3155 (2001)

[81] S. M. Huang, M. Woodson, R. Smalley, and J. Liu, *Nano Lett.* **4**, 1025 (2004).

[82] Z. Jin, H. B. Chu, J. Y. Wang, J. X. Hong, W. C. Tan, and Y. Li, *Nano Lett.* **7**, 2073 (2007).

[83] A. Ismach, L. Segev, E. Wachtel, and E. Joselevich, *Angew. Chem. Int. Ed.* **43**, 6140 (2004).

[84] L. Ding, D. N. Yuan, and J. Liu, *J. Am. Chem. Soc.* **130**, 5428 (2008).

[85] Z. F. Ren, Z. P. Huang, J. W. Xu, J. H. Wang, P. Bush, M. P. Siegal, and P. N. Provencio, *Science* **282**, 1105 (1998).

[86] A. V. Melechko, V. I. Merkulov, T. E. McKnight, M. A. Guillorn, K. L. Klein, D. H. Lowndes, and M. L. Simpson, *J. Appl. Phys.* **97**, 041301 (2005).

[87] A. B. Kaul, K. Megerian, P. von Allmen, and R. L. Baron, *Nanotechnology* **20**, 075303 (2009).

[88] M. C. Hersam, *Nat. Nanotechnol.* **3**, 387 (2008).

[89] L. Ding, A. Tselev, J. Wang, D. Yuan, H. Chu, T. P. McNicholas, Y. Li, and J. Liu, *Nano Lett.* **9**, 800 (2009).

[90] S. Hung, A. Javey, J. Cao, D. Wang, E. Yenilmez, Q. Wang, J. F. Gibbons, Y. Nishi, and H. Dai, *Nano Lett.* **4**, 317 (2004).

[91] L. An, Q. Fu, C. Lu, and J. Liu, *J. Am. Chem. Soc.* **126**, 10520 (2004).

[92] G. Y. Zhang, P. F. Qi, X. R. Wang, Y. R. Lu, S. L. Li, R. Tu, S. Bangsaruntip, D. Mann, L. Zhang, and H. J. Dai, *Science* **314**, 974 (2006).

[93] H. J. Huang, R. Maruyama, K. Noda, H. Kajiura, and K. Kadono, *J. Phys. Chem. B* **110**, 7316 (2006).

[94] Y. Y. Zhang, Y. Zhang, X. J. Xian, J. Zhang, and Z. F. Liu, *J. Phys. Chem.* **112**, 3849 (2008).

[95] H. Shim, J. Song, Y. Kwak, S. Kim, and C. Han, *Nanotech.* **20**, 065707 (2009).

[96] P. C. Collins, M. S. Arnold, and P. Avouris, *Science* **292**, 706 (2001).

[97] J. Kong, E. Yenilmez, T. W. Tombler, W. Kim, and H. Dai, *Phys. Rev. Lett.* **87**, 106801-1 (2001).

[98] S. Frank, P. Poncharal, Z.L. Wang, and W. A. de Heer, *Science* **280** (1998).

[99] Y. Zhang, N. Franklin, R. Chen, and H. Dai, *Chem. Phys. Lett.* **331**, 425 (2000).

[100] R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K. K. Chan, J. Tersoff, and P. Avouris, *Phys. Rev. Lett.* **87**, 256805-1 (2001).

[101] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. J. Dai, *Nature* **424**, 654 (2003).

[102] S. Ahmed, S. Das, M.K. Mitra, and K. K. Chattopadhyay *Appl. Surf. Sci.* **254**, 610 (2007).

[**103**] D. Mann, A. Javey, J. Kong, Q. Wang, and H. Dai, *Nano Lett.* **3**, 1541 (2003).

[**104**] S. C. Lim, J. h. Jang, D. J. Bae, G. H. Han, s. Lee, I. Yeo, and Y. Lee, *Appl. Phys. Lett.* **95**, 264103 (2009).

[**105**] C. Dekker, *Physics Today* **52**, 22 (1999).

[**106**] S. J. Tans, M. Devoret, H. Dai, A. Thess, R. Smalley, L. Geerligs, and C. Dekker, *Nature* **386**, 474 (1997).

[**107**] M. Bockrath, D. Cobden, J. Lu, A. Rinzler, R. Smalley, L. Balents, and P. McEuen, *Nature* **397**, 598 (1999).

[**108**] H. Ishikuro and T. Hiramoto, *Appl. Phys. Lett.* **68**, 3585 (1996).

[**109**] Y. A. Pashkin, Y. Nakamura, and J. S. Tsai, *Appl. Phys. Lett.* **68**, 34 (1996).

[**110**] J. Nygard, D. H. Cobden, M. Bockrath, P. L. McEuen, and P. E. Lindelof, *Appl. Phys. A* **69**, 297 (1999).

[**111**] M. Bockrath, D. Cobden, P. McEuen, N. Chopra, A. Zettl, A. Thess, R. Smalley, *Science* **275**, 1922 (1997).

[**112**] H. B. Peng, J. A. Golovchenko, *Appl. Phys. Lett.* **84**, 5428 (2004).

[**113**] R. S. Lee, H. J. Kim, J. E. Fischer, A. Thess, R. E. Smalley, *Nature* **388**, 255 (1997).

[**114**] L. Grigorian, K. Williams, S. Fang, G. Sumanasekera, A. Loper, E. Dickey, S. Pennycook, and P. Eklund, *Phys. Rev. Lett.* **80**, 5560 (1998).

[**115**] M. Bockrath, J. Hone, A. Zettl, P. McEuen, A. Rinzler, and R. Smalley, *Phys. Rev. B* **61**, R10606 (2000).

[**116**] J. Kong, C. Zhou, E. Yenilmez, and H. Dai, *Appl. Phys. Lett.* **77**, 3977 (2000).

[**117**] M. Burghard, H. Klauk, and K. Kern, *Adv. Mater.* **21**, 2586 (2009).

[**118**] S. J. Tans, A. R. M. Verschueren, and C. Dekker, *Nature* **393**, 49 (1998).

[**119**] S. Wind, J. Appenzeller, R. Martel, V. Derycke, and P. Avouris, *Appl. Phys. Lett.* **80**, 3817 (2002).

[**120**] A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, and H. J. Dai, *Nat. Mater.* **1**, 241 (2002).

[**121**] A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. W. Wang, R. G. Gordon, M. Lundstrom, and H. J. Dai, *Nano Lett.* **4**, 447 (2004).

[**122**] M. H. Yang, K. B. K. Teo, L. Gangloff, W. I. Milne, D. G. Hasko, Y. Robert, and P. Legagneux, *Appl. Phys. Lett.* **88**, 113507 (2006).

[**123**] Y. R. Lu, S. Bangsaruntip, X. R. Wang, L. Zhang, Y. Nishi, and H. J. Dai, *J. Am. Chem. Soc.* **128**, 3518 (2006).

[**124**] R. T. Weitz, U. Zschieschang, F. Effenberger, H. Klauk, M. Burghard, and K. Kern, *Nano Lett.* **7**, 22 (2007).

[**125**] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, *Phys. Rev. Lett.* **89**, 106810 (2002).

[**126**] V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, *Nano Lett.* **1**, 453 (2001).

[**127**] S. M. Lee, Y. H. Lee, Y. G. Hwang, J. R. Hahn, and H. Kang, *Phys. Rev. Lett.* **82**, 217 (1999).

[**128**] A. Javey, Q. Wang, A. Urai, Y. Li, and H. Dai, *Nano Lett.* **2**, 929 (2002).

[**129**] S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, and J. A. Rogers, *Nat. Nanotechnol.* **2**, 230 (2007).

[**130**] Q. Cao, H. s. Kim, N. Pimparkar, J. P. Kulkarni, C. J. Wang, M. Shim, K. Roy, M. A. Alam, and J. A. Rogers, *Nature* **454**, 495 (2008).

[**131**] J. E. Baumgardner, A. A. Pesetski, J. M. Murduck, J. X. Przybysz, J. D. Adam, and H. Zhang, *Appl. Phys. Lett.* **91**, 052107 (2007).

[**132**] C. Rutherglen, D. Jain, and P. Burke, *Nature Nanotechnol.* **4**, 811 (2009).

[**133**] Z. H. Chen, J. Appenzeller, Y. M. Lin, J. S. Oakley, A. G. Rinzler, J. Y. Tang, S. J. Wind, P. M. Solomon, and P. Avouris, *Science* **311**, 1735 (2006).

[**134**] D. Wang, Z. Yu, S. McKernan, and P. Burke, *IEEE Trans. Nanotech.* **6**, 400 (2007).

[**135**] C. Kocabas, S. Dunham, Q. Cao, K. Cimino, X. N. Ho, H. S. Kim, D. Dawson, J. Payne, M. Stuenkel, H. Zhang, T. Banks, M. Feng, S. V. Rotkin, and J. A. Rogers, *Nano Lett.* **8**, 1937 (2009).

[**136**] L. Nougaret, H. Happy, G. Dambrine, V. Derycke, J. P. Bourgoin, A. A. Green, and M. C. Hersam, *Appl. Phys. Lett.* **94**, 243505 (2009).

[**137**] A. Le Louarn, F. Kapache, J. M. Bethoux, H. Happy, G. Dambrine, V. Derycke, P. Chenevier, N. Izard, M. F. Goffman, and J. P. Bourgoin, *Appl. Phys. Lett.* 90, 233108 (2007).

[**138**] C. Kocabas, H. S. Kim, T. Banks, J. A. Rogers, A. A. Pesetski, J. E. Baumgardner, S. V. Krishnaswamy, and H. Zhang, *Proc. Natl. Acad. Sci. USA* **105**, 1405 (2008).

[**139**] C. Rutherglen and P. Burke, *Nano Lett.* **7**, 3296 (2007).

[**140**] K. Jensen, J. Weldon, H. Garcia, and A. Zettl, *Nano Lett.* **7**, 3508 (2007).

[**141**] A. Naeemi and J. Meindl, *Annu. Rev. Mater. Res.* **39**, 255 (2009).

[**142**] W. Steinhogl, G. Schindler, G. Steinlesberger, M. Traving, and M. Engelhardt, *J. Appl. Phys.* 97, 023706 (2005).

[**143**] P. L. McEuen, M. S. Fuhrer, and H. Park, *IEEE Trans. Nanotech.* **1**, 78 (2002).

[**144**] A. Naeemi and J. D Meindl, *IEEE Trans. Electron Dev.* **55**, 2574 (2008).

[**145**] A. Nieuwoudt and Y. Massoud, *IEEE Trans. Nanotechnol.* **5**, 758 (2006).

[**146**] M. W. Bockrath, Carbon nanotubes: electrons in one dimension. Ph.D. Thesis, University of California, Berkeley (1999).

[**147**] J. J. Plombon, K. P. O'Brien, F. Gstrein, V. M. Dubin, and Y. Jiao, *Appl. Phys. Lett.* **90**, 063106 (2007).

[**148**] H. Li and K. Banerjee, *IEEE Trans. Elec. Dev.* **5**6, 2201 (2009).

[**149**] A. Naeemi and J. D. Meindl, *IEEE Elect. Dev. Lett.* **27**, 338 (2006).

[**150**] S. S. Fan, M. G. Chapline, N. R. Franklin, T. W. Tombler, A. M. Casssell, and H. J. Dai, *Science* **283**, 512 (1999).

[**151**] D. N. Futaba, K. Hata, T. Namai, T. Yamada, K. Mizuno, Y. Hayamizu, M. Yumura, and S. Iijima, *J. Phys. Chem. B* **110**, 8035 (2006).

[**152**] D. N. Futaba, K. Hata, T. Yamada, T. Hiraoka, Y. Hayamizu, Y. Kakudate, O. Tanaike, H. Hatori, M. Yumura, and S. Iijima, *Nat. Materials* **5**, 987 (2006).

[**153**] Y. Maeda, S. Kimura, M. Kanda, Y. Hirashima, T. Hasegawa, T. Wakahara, Y. Lian, T. Nakahodo, T. Tsuchiya, T. Akasaka, J. Lu, X. Zhang, C. Gao, Y. Yu, S. Nagase, S. Kazaoui, N. Kinami, T. Shimizu, H. Tokumoto, and R. Saito, *J. Amer. Chem. Soc.* **127**, 10287 (2005).

[**154**] S. Talapatra, S. Kar, S. K. Pal, R. Vajtai, L. Ci, P. Victor, M. M. Shaijumon, S. Kaur, O. Nalamasu, and P. M. Ajayan, *Nat. Nanotechnol.* **1**, 112 (2006).

[**155**] Y. Awano, S. Sato, D. Kondo, M. Ohfuti, A. Kawabata, M. Niehei, N. Yokoyama, *Phys. Status Solidi A* **203**, 3611 (2006).

[**156**] M. Cantoro, S. Hofmann, S. Pisana, V. Scardaci, A. Parvez, C. Ducati, A. C. Ferrari, A. M. Blackburn, K. Y. Wang, and J. Robertson, *Nano Lett.* **6**, 1107 (2006).

[**157**] S. Huang, X. Cai, and J. Liu, *J. Amer. Chem. Soc.* **125**, 5636 (2003).

[**158**] H. Xin and A. T. Woolley, *Nano Lett.* **4**, 1481 (2004).

[**159**] L. Zhu, J. Xu, Y. Xiu, Y. Sun, D. W. Hess, and C. P. Wong, *Carbon* **44**, 253 (2006).

[**160**] T. Xu, Z. Wang, J. Miao, X. Chen, and C. M. Tan, *Appl. Phys. Lett.* **91**, 042108 (2007).

[**161**] R. H. Baughman, A.A. Zakhidov, and W.A. de Heer, *Science* **297**, 787 (2002).

[**162**] J.A. Nichols, H. Saito, C. Deck, and P.R. Bandaru, *J. Appl. Phys.* **102**, 064306 (2007).

[**163**] Y. Fan, B.R. Goldsmith, and P.G. Collins, *Nature Materials* 4, 906 (2005).

[**164**] P.L. McEuen, *Nature* **393**, 15 (1998).

[**165**] P. Castrucci, M. Scarselli, M. De Crescenzi, M. A. El Khakani, F. Rosei, N. Braidy, and J.-H. Yi, *Appl. Phys. Lett.*, **85**, 3857 (2004).

[**166**] M.S. Dresselhaus, G. Dresselhaus, and A. Jorio, *Ann. Rev. Mat. Res.* **34**, 247 (2004).

[**167**] H. Dai, *Acc. Chem. Res.* **35**, 1035 (2002).

[**168**] P.M. Ajayan, *Chem. Rev.* **99**, 1787 (1999).

[**169**] P.R. Bandaru, *J. Nanosci. & Nanotech.* **7**, 1239 (2007).

[**170**] R. Saito, G. Dresselhaus, and M.S. Dresselhaus, *Physical Properties of Carbon Nanotubes*. (Imperial College Press, London, 1998).

[**171**] Z. Yao, H. W. Ch. Postma, L. Balents, and C. Dekker, *Nature* **402**, 273 (1999).

[**172**] P.G. Collins and P. Avouris, *Scientific American*, 62 (December, 2000).

[**173**] J. Hone, M.C. Laguno, N.M. Nemes, A.T. Johnson, J.E. Fischer, D.A. Walters, M.J. Casavant, J. Schmidt, and R.E. Smalley, *Appl. Phys. Lett.* **77**, 666 (2000).

[**174**] C.T. White and T.N. Todorov, *Nature* **393**, 240 (1998).

[**175**] M. Buitelaar, T. Nussbaumer, A. Bachtold, M. Iqbal, and C. Schönenberger, *Phys. Rev. Lett.* **88**, 156801 (2002).

[**176**] P. Delaney, M. Di Ventra, and S. Pantelides, *Appl. Phys. Lett.* **75**, 3787 (1999).

[**177**] H. W. Ch. Postma, T. Teepen, Z. Yao, M. Grifoni, and C. Dekker, *Science* **293**, 76 (2001).

[**178**] M. Freitag, M. Radosavljevic, Y. Zhou, and A.T. Johnson, *Appl. Phys. Lett.* **79**, 3326 (2001).

[**179**] M. Radosavljevic, M. Freitag, K.V. Thadani, and A.T. Johnson, Non-volatile molecular memory elements based on ambipolar nanotube field effect transistors, *arxiv:cond-mat/0206392* (2002).

[**180**] R. Martel, V. Derycke, J. Appenzeller, S. Wind, and P. Avouris, presented at the Design Automation Conference, ACM, New Orleans, LA, 2002 (unpublished).

[**181**] P.G. Collins, M. Hersam, M. Arnold, R. Martel, and P. Avouris, *Phys. Rev. Lett.* **86**, 3128 (2001).

[**182**] P. Kim, L. Shi, A. Majumdar, and P.L. McEuen, *Phys. Rev. Lett.* **87**, 215502 (2001).

[**183**] J.O. Wesstrom, *Phys. Rev. Lett.* **82**, 2564 (1999).

[**184**] S. Iijima, T. Ichihashi, and Y. Ando, *Nature* **356**, 776 (1992).

[**185**] M. Terrones, F. Banhart, N. Grobert, J.-C. Charlier, H. Terrones, and P.M. Ajayan, *Phys. Rev. Lett.* **89**, 075505 (2002).

[**186**] W.Z. Li, J.G. Wen, and Z.F. Ren, *Appl. Phys. Lett.* **79**, 1879 (2001).

[187] C. Papadapoulos, A. Rakitin, J. Li, A.S. Vedeneev, and J.M. Xu, *Phys. Rev. Lett.* **85**, 3476 (2000).

[188] B.C. Satishkumar, P.J. Thomas, A. Govindaraj, and C.N.R. Rao, *Appl. Phys. Lett.* **77**, 2530 (2000).

[189] D. Zhou and S. Seraphin, *Chem. Phys. Lett.* **238**, 286 (1995).

[190] J-M. Ting and C-C. Chang, *Appl. Phys. Lett.* **80**, 324 (2002).

[191] M.S. Fuhrer, J. Nygard, L. Shih, M. Forero, Y-G. Yoon, M.S.C. Mazzoni, H. J. Choi, J. Ihm, S. Louie, A. Zettl, and P.L. McEuen, *Science* **288**, 494 (2000).

[192] N. Gothard, C. Daraio, J. Gaillard, R. Zidan, S. Jin, and A.M. Rao, *Nano Lett.* **4** (2), 213 (2004).

[193] K. B. K. Teo, C. Singh, M. Chhowalla, and W.I. Milne, in *Encyclopedia of Nanoscience and Nanotechnology*, edited by H.S. Nalwa (American Scientific Publishers, Stevenson Ranch, CA, 2004).

[194] Y.C. Choi and W. Choi, Synthesis of Y-junction single-wall carbon nanotubes, *Carbon* **43**, 2737 (2005).

[195] P.R. Bandaru, C. Daraio, K. Yang, and A.M. Rao, *J. Appl. Phys.* **101**, 094307 (2007).

[196] H. Dai, in *Topics in Applied Physics*, edited by M.S. Dresselhaus, G. Dresselhaus, and P. Avouris (Springer-Verlag, Berlin, 2001), Vol. 80, pp. 29.

[197] L. Forro and C. Schonenberger, in *Carbon Nanotubes- Topics in Applied Physics*, edited by M.S. Dresselhaus, G. Dresselhaus, and P. Avouris (Springer-Verlag, Heidelberg, 2001), Vol. 80.

[198] A. Bachtold, C. Strunk, J-P. Salvetat, J-M. Bonard, L. Forro, T. Nussbaumer, and C. Schonenberger, *Nature* **397**, 673 (1999).

[199] K. Tsukagoshi, E. Watanabe, I. Yagi, N. Yoneya, and Y. Aoyagi, *New J. Phys.* **6**, 1 (2004).

[200] T. Palm and L. Thylen, *Appl. Phys. Lett.* **60**, 237 (1992).

[201] L. Worschech, H.Q. Xu, A. Forchel, and L. Samuelson, *Appl. Phys. Lett.* **79**, 3287 (2001).

[202] R. Lewen, I. Maximov, I. Shorubalko, L. Samuelson, L. Thylen, and H.Q. Xu, *J. Appl. Phys.* **91**, 2398 (2002).

[203] K. Hieke and M. Ulfward, *Phys. Rev. B* **62**, 16727 (2000).

[204] I. Shorubalko, H.Q. Xu, P. Omling, and L. Samuelson, *Appl. Phys. Lett.* **83**, 2369 (2003).

[205] A.M. Song, A. Lorke, A. Kriele, J.P. Kotthaus, W. Wegscheider, and M. Bichler, *Phys. Rev. Lett.* **80**, 3831 (1998).

[206] A.N. Andriotis, M. Menon, D. Srivastava, and L. Chernozatonski, *Phys. Rev. Lett.* **87** (6), 066802 (2001).

[207] A.N. Andriotis, D. Srivastava, and M. Menon, *Appl. Phys. Lett.* **83**, 1674 (2003).

[**208**] W. Tian, S. Datta, S. Hong, R. Reifenberger, J.I. Henderson, and C.P. Kubiak, *J. Chem. Phys.* **109**, 2874 (1998).

[**209**] V. Meunier, M.B. Nardelli, J. Bernholc, T. Zacharia, and J.-C. Charlier, *Appl. Phys. Lett.* **81**, 5234 (2002).

[**210**] G.E. Scuseria, *Chem. Phys. Lett.* **195**, 534 (1992).

[**211**] A.N. Andriotis, M. Menon, D. Srivastava, and L. Chernozatonski, *Phys. Rev. B* **65**, 165416 (2002).

[**212**] J.H. Davies, *The Physics of Low-Dimensional Semiconductors*. (Cambridge University Press, New York, 1998)

[**213**] H.Q. Xu, *Appl. Phys. Lett.* **80**, 853 (2001).

[**214**] D. Csontos and H.Q. Xu, *Phys. Rev. B* **67**, 235322 (2003).

[**215**] H.Q. Xu, *Physica E* **13**, 942 (2002).

[**216**] T. Palm and L. Thylen, *J. Appl. Phys.* **79**, 8076 (1996).

[**217**] V.H. Crespi, *Phys. Rev. B* **58**, 12671 (1998).

[**218**] A.M. Song, P. Omling, L. Samuelson, W. Seifert, I. Shorubalko, and H. Zirath, *Appl. Phys. Lett.* **79**, 1357 (2001).

[**219**] D-H. Kim, J. Huang, H-K. Shin, S. Roy, and W. Choi, *Nano Lett.* **6**, 2821 (2006).

[**220**] V. Gopal, V.R. Radmilovic, C. Daraio, S. Jin, P. Yang, and E.A. Stach, *Nano Letters* **4**, 2059 (2004).

[**221**] B.R. Perkins, D.P. Wang, D. Soltman, A.J. Yin, J.M. Xu, and A. Zaslavsky, *Appl. Phys. Lett.* **87**, 123504 (2005).

[**222**] H.Q. Xu, *Appl. Phys. Lett.* **78** (14), 2064 (2001).

[**223**] D. Wallin, I. Shorubalko, H.Q. Xu, and A. Cappy, *Appl. Phys. Lett.* ***89***, 092124 (2006).

[**224**] H.Q. Xu, *Appl. Phys. Lett.* **80**, 853 (2002).

[**225**] J.W. Ding, X.H. Yan, and J.X. Cao, *Phys. Rev. B: Condens. Matter* **66**, 073401 (2002).

[**226**] A.N. Andriotis and M. Menon, *Appl. Phys. Lett.* **89**, 132116 (2006).

[**227**] M. Beale and P. Mackay, *Phil. Mag. B* **65**, 47 (1992).

[**228**] M.H. Yang, K. B. K. Teo, W.I. Milne, and D.G. Hasko, *Appl. Phys. Lett.* **87**, 253116 (2005).

[**229**] H.M. Manohara, E.W. Wong, E. Schlecht, B.D. Hunt, and P.H. Siegel, *Nano Lett.* **5**, 1469 (2005).

[**230**] J.U. Lee, P.P. Gipp, and C.M. Heller, *Appl. Phys. Lett.* **85**, 145 (2004).

[**231**] Y. Zhang, N.W. Franklin, R.J. Chen, and H. Dai, *Chem. Phys. Lett.* **331**, 35 (2000).

[232] J. Appenzeller, J. Knoch, R. Martel, and V. Derycke, *IEEE Trans. Nanotech.* **1**, 184 (2002).

[233] M. Freitag, Y. Martin, J.A. Misewich, R. Martel, and P. Avouris, *Nano Lett.* **3**, 1067 (2003).

[234] P.M. Ajayan, T.W. Ebbesen, T. Ichihashi, S. Ijima, K. Tanigaki, and H. Hiura, *Nature* **362**, 522 (1993)

[235] R.S. Muller and T.I. Kamins, *Device Electronics for Integrated Circuits*, 2 ed. (John Wiley, New York, 1986)

[236] R.D. Antonov and A.T. Johnson, *Phys. Rev. Lett.* **83**, 3274 (1999).

[237] W. Shockley, *Electrons and Holes in Semiconductors*. (Princeton, New Jersey, 1950).

[238] B.G. Streetman and S. Banerjee, *Solid State Electronic Devices*, 5 ed. (Prentice Hall, New Jersey, 2000).

[239] S.M. Sze, *Physics of Semiconductor Devices*, 2 ed. (John Wiley, New York, 1981).

[240] J. Park, C. Daraio, S. Jin, P.R. Bandaru, J. Gaillard, and A.M. Rao, *Appl. Phys. Lett.* **88**, 243113 (2006).

[241] J. Rabaey, *Digital Integrated Circuits: A Design Perspective*. (Prentice Hall, New York, 1996).

[242] P.J. Burke, *IEEE Trans. Nanotech.* **2** (1), 55 (2003).

[243] P.J. Burke, *IEEE Trans. Nanotech.* **1**, 129 (2002).

[244] J. Guo, S. Datta, M. Lundstrom, Brink. M., P.L. McEuen, A. Javey, H. Dai, H. Kim, and P. McIntyre, presented at the International Electron Devices Meeting (IEDM), San Francisco, CA, 2002 (unpublished)

[245] H.Q. Xu, *Nature Materials* **4**, 649 (2005).

[246] H. Kosaka, D.S. Rao, H. Robinson, P.R. Bandaru, T. Sakamoto, and E. Yablonovitch, *Phys. Rev. B (Rapid Communications)* **65**, 201307 (2002).

[247] X.M.H. Huang, R. Caldwell, L. Huang, S.C. Jun, M. Huang, M.Y. Sfeir, S.P. O'Brien, and J. Hone, *Nano Lett.* **5**, 1515 (2005).

[248] J. Liu, M.J. Casavant, M. Cox, D.A. Walters, P. Boul, W. Lu, A.J. Rimberg, K.A. Smith, D. Colbert, and R.E. Smalley, *Chem. Phys. Lett.* **303**, 125 (1999).

[249] S.G. Rao, L. Huang, W. Setyawan, and S. Hong, *Nature* **425**, 36 (2003).

[250] Y. Huang, X. Duan, Q. Wei, and C. M. Lieber, *Science* **291**, 630 (2001).

[251] L. Qin, S. Park, L. Huang, and C.A. Mirkin, *Science* **309**, 113 (2005).

[252] P. R. Wallace, *Phys. Rev.* 71, 622 (1947).

[253] J. W. Evans, P. A. Thiel, and M. C. Bartelt, *Sur. Sci. Rep.* **61**, 1 (2006).

[254] R. E. Peierls, *Ann. I. H. Poincare* **5**, 177 (1935).

[255] K. S. Novoselov, D. Jiang, F. Schedin, T. J. Booth, V. V. Khotkevicy, S. V. Morozov, A. K. Geim, *Proc. Natl. Acad. Sci. USA* **102**, 10451 (2005).

[256] A. K. Geim and K. S. Novoselov, *Nat. Mater.* **6**, 183 (2007).

[257] A. C. Ferrari, J. C. Meyer, V. Scardaci, C. Casiraghi, M. Lazzeri, F. Mauri, S. Piscanec, D. Jiang, K. S. Novoselov, S. Roth, A. K. Geim, *Phys. Rev. Lett.* 97, 187401 (2006).

[258] Y. W. Son, M. L. Cohen, and S. G. Louie, *Phys. Rev. Lett.* **97**, 216803 (2006).

[259] S. V. Morozov, K. S. Novoselov, F. Schedin, D. Jiang, A. A. Firsov, and A. K. Geim, *Phys. Rev. B* **72**, 201401 (2005).

[260] B. Partoens and F. M. Peeters, *Phys. Rev. B* **74,** 075404 (2006).

[261] F. Schedin, A. K. Geim, S. V. Morozov, E. W. hill, P. Blake, M. I. Katsnelson, and K. S. Novoselov, *Nature Materials* **6**, 652 (2007).

[262] J. C. Meyer, A. K. Geim, M. I. Katsnelson, K. S. Novoselov, T. J. Booth, and S. Roth, *Nature* **446**, 60 (2007).

[263] J. S. Bunch, A. M. van der Zande, S. S. Verbridge, I. W. Grank, D. M. Tanenbaum, J. M. Parpia, H. G. Craighead, and P. L. McEuen, *Science* **315**, 490 (2007).

[264] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, *Solid State Communications*, 146, 351 (2008).

[265] J. B. Oostinga, H. B. Heersche, X. L. Liu, A. F. Morpurgo, and L. M. K. Vandersypen, *Nat. Mater.* **7**, 151 (2008).

[266] E. V. Castro, K. S. Novoselov, S. V. Mrozov, N. M. R. Peres, J. M. B. L. Dos Santos, J. Nilsson, F. Guinea, A. K. Geim, and A. H. C. Neto, *Phys. Rev. Lett.* **99**, 216802 (2007).

[267] V. Barone, O. Hod, and G. E. Scuseria, *Nano Lett.* **6**, 2748 (2006).

[268] B. D. Josephson, *Phys. Lett.* **1**, 251 (1962).

[269] H. B. Heersche, P. J. Herrero, J. B. Oostinga, L. M. K. Vandersypen and A. F. Morpurgo, *Nature* **446**, 56 (2007).

[270] C. Lee, X. Wei, J. W. Kysar, and J. Hone, *Science* **321**, 385 (2008).

[271] O. Hod and G. E. Scuseria, *Nano Lett.* **9**, 2619 (2009).

[272] L. Sun, Q. Li, H. Ren, H. Su, Q. W. Shi, and J. Yang, *J. Chem. Phys.* **129**, 074704 (2008).

[273] K. S. Novoselov, E. McCann, S. V. Morozov, V. I. Falko, M. I. Katsnelson, U. Zeitler, D. Jiang, F. Schedin, and A. K. Geim, *Nat. Phys.* **2**, 177 (2006).

[274] http://www.grapheneindustries.com

[**275**] S. Stankovich, D. A. Dikin, G. H. B. Dommett, K. M. Kohlhass, E. J. Zimney, E. A. Stach, R. D. Piner, S. T. Nguyen, and R.S. Ruoff, *Nature* **442**, 282 (2006).

[**276**] S. Stankovich, D. A. Dikin, R. D. Piner, K. A. Kohnhass, A. Kleinhammes, Y. Jia, Y. Wu, S. T. Nguyen, and R.S. Ruoff, *Carbon* **45**, 1558 (2007).

[**277**] K. N. Kudin, B. Ozbas, H. C. Schniepp, R. K. Prudhomme, I. A. Aksay, and R. Car, *Nano Lett.* **8**, 36 (2008).

[**278**] C. Berger, Z. Song, X. Li, X. Wu, N. Brown, C. Naud, D. Mayouu, T. Li, J. Hass, A. N. Marchenkov, E. H. Conrad, P. N. First, W. A. de Heer, *Science* **312**, 1191 (2006).

[**279**] J. Hass, R. Feng, T. Li, X. Li, Z. Zong, W. A. de Heer, P. N. First, E. H. Conrad, C. A. Jeffery, and C. Berger, *Appl. Phys. Lett.* **89**, 143106 (2006).

[**280**] G. M. Rutter, J. N. Crain, N. P. Guisinger, T. Li, P. N. First, J. A. Stroscio, *Science* **317**, 219 (2007).

[**281**] J. Coraux, A. T. NDiaye, C. Busse, and T. Michely, *Nano Lett.* **8**, 565 (2008).

[**282**] S. Marchini, S. Gunther, and J. Wintterlin, *J. Phys. Rev. B* **76**, 075429 (2007).

[**283**] M. Ezawa, *Phys. Rev. B*, **73**, 045432 (2006).

[**284**] L. Brey and H. A. Fertig, *Phys. Rev. B.* **73**, 235411 (2006).

[**285**] P. Shemella, Y. Zhang, M. Mailman, P. M. Ajayan, and S. K. Nayak, *Appl. Phys. Lett.* **91**, 042101 (2007).

[**286**] Y. W. Son, M. L. Cohen, and S. G. Louie, *Nature* **444**, 347 (2006).

[**287**] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, *Science* **319**, 1229 (2008).

[**288**] X. R. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, *Phys. Rev. Lett.* **100**, 206803 (2008).

[**289**] A. Tomita and Y. J. Tamai, *J. Phys. Chem.* **78**, 2254 (1974).

[**290**] S. Datta, D. Strachan, S. M. Khamis, and A. T. C. Johnson, *Nano Lett.* **8**, 1912 (2008).

[**291**] H. T. Ng, J. Li, M. K. Smith, P. Nguyen, A. Cassel, J. Han, and M. Meyyappan, *Science* **300**, 1249 (2003).

[**292**] P. Kim and C. M. Lieber, *Science* **286**, 2148-2150 (1999).

[**293**] E. Dujardin, V. Derycke, and M. F. Goffman, *Appl. Phys. Lett.* **87**, 193107 (2005).

[**294**] Z. Chen, L. Tong, Z. Wu, and Z. Liu, *Appl. Phys. Lett.* **92**, 103116 (2008).

[**295**] A. Eriksson, S. Lee, A. A. Sourab, A. Isacsson, R. Kaunisto, J. M. Kinaret, and E. E. B. Campbell, *Nano Lett.* **8**, 1224 (2008).

[**296**] D. A. Walters, L. M. Ericson, M. J. Casavant, J. Liu, D. T. Colbert, K. A. Smith, and R. E. Smalley, *Appl. Phys. Lett.* **74**, 3803 (1999).

[**297**] T. Tombler, C. Zhou, L. Alexseyev, J. Kong, H. Dai, L. Liu, C. S. Jayanthi, M. Tang, and S. Wu, *Nature* **405**, 769 (2000).

[**298**] E. D. Minot, Y. Yaish, V. Sazonova, J. Y. Park, M. Brink, and P. L. McEuen, *Phys. Rev. Lett.* **90**, 156401-1 (2003).

[**299**] A. B. Kaul and H. Manohara, *IEEE Trans. Nanotech.* **8**, 252 (2009).

[**300**] A. B. Kaul, *Nanotech.* **20**, *155501* (2009).

[**301**] J. Nygard, D. H. Cobden , *Appl. Phys. Lett.* **79**, 4216 (2001).

[**302**] S. N. Cha, J. E. Jang, Y. Choi, G. A. J. Amaratunga, D. J. Kang, D. G. Hasko, J. E. Jung, and J. M. Kim *Appl. Phys. Lett.* **86**, 083105 *(*2005).

[**303**] S. W. Lee, D. S. Lee, R. E. Morjan, S. H. Jhang, M. Sveningsson, O. A. Nerushev, Y. W. Park, and E. E. B. Campbell, *Nano. Lett.* **4**, 2027 (2004).

[**304**] J. E. Jang, S. N. Cha, Y. Choi, G. A. J. Amaratunga, D. J. Kang, D. G. Hasko, J. E. Jung, and J. M. Kim *Appl. Phys. Lett.* **87**, 163114 (2005).

[**305**] A. B. Kaul, A. Khan, L. Bagge, K. G. Megerian, H. G. LeDuc, and L. Epp, *Appl. Phys. Lett.* **95**, 093103, (2009).

[**306**] S. Ahmed, S. Das, M. K. Mitra, and K. K. Chattopadhyay, *Appl. Surf. Sci.*, 254, 610 (2007).

[**307**] Y. Saito, S. Kawata, H. Nakane, and H. Adachi, *Appl. Surf. Sci.* **146**, 177 (1999).

[**308**] M. Dequesnes, S. V. Rotkin, and N. R. Aluru, *Nanotech.* **13**, 120 (2002).

[**309**] Nantero, Inc: http://www.nantero.com/

[**310**] Y. Hayamizu, T. Yamada, K. Mizuno, R. C. Davis, D. N. Futaba, M. Yumura, and K. Hata, *Nat. Nanotech.* **3**, 289 (2008).

[**311**] B. Ilic, Y. Yang, and H. G. Craighead, *Appl. Phys. Lett.* **85**, 2604 (2004).

[**312**] A. Naik, M. Hanay, W. Hiebert, X. Feng, and M. Roukes, *Nature Nanotech.* 4, 445 (2009).

[**313**] V. Sazonova, Y. Yaish, H. Ustunel, D. Roundy, T. A. Arias, and P. L. McEuen, *Nature* **431**, 284 (2004).

[**314**] H. B. Peng, C. Chang, S. Aloni, T. D. Yuzvinsky, and A. Zettl, *Phys. Rev. Lett.* **97**, 087203 (2006).

[**315**] R. J. Grow, Q. Wang, J. Cao, D. Wang, and H. Dai, *Appl. Phys. Lett.* **86**, 093104 (2005).

[**316**] C. Stampfer, T. Helbling, D. Obergfell, B. Schoberle, M. K. Tripp, A. Jungen, S. Roth, V. M. Bright, and C. Hierold, *Nano Lett.* **6**, 233 (2006).

[**317**] T. Kawano, H. C. Chiamori, M. Suter, Q. Zhou, B. D. Sosnowchik, and L. W. Lin, *Nano Lett.* **7**, 3686 (2007).

[**318**] T. Kawano, D. Christensen, S. Chen, C. Cho, and L. Lin, *Appl. Phys. Lett.* **89**, 163510 (2006).

[**319**] K. E. Peterson, *Proc. IEEE* **70**, 420 (1982).

[**320**] M. Esashi, S. Sugiyama, K. Ikeda, Y. Wang, and H. Miyashita, *Proc. IEEE* **86**, 1627 (1998).

[**321**] W. J. Alvesteffer, D. Jacobs, and D. H. Baker, *J. Vac. Sci. Technol. A* **13**, 2980 (1999).

[**322**] E. Pop, D. Mann, J. Cao, Q. Wang, K. Goodson, and H. J. Dai, *Phys. Rev. Lett.*, **95**, 155505 (2005).

[**323**] G. E. Moore, *Elect. Lett.* **38,** 4 (1965).

[**324**] *Nanosilicon* edited by V. Kumar (Elsevier Inc., San Diego, CA, 2008).

[**325**] W. Hu, F. Yoon, S. Regonda, P. Fernandes, E. M. Vogel, F. Buyukserin, X.-M. Zhao, and J. Gao, , *IEEE Int. Conf. Nanotech., IEEE NANO 2008* (2008).

[**326**] L. R. Harriott, in *SCALPEL: Projection electron beam lithography, Proc. 1999 Particle Accel. Conf.,* New York, 1999.

[**327**] A. A. Tseng, K. Chen, C. D. Chen, and K. J. Ma, *IEEE Trans. Elec. Pack. & Manuf.* **26,** 141 (2003).

[**328**] N. A. Melosh, A. Boukai, F. Diana, B. Gerardot, A. Badolato, P. M. Petroff, and J. R. Heath, *Science* **300,** 112 (2003).

[**329**] K. J. Morton, G. Nieberg, S. Bai, and S. Y. Chou, *Nanotechnology* **19,** 345301 (2008).

[**330**] J. R. Heath, *Acc. Chem. Res.* **41,** 1609 (2008).

[**331**] A. I. Boukai, Y. Bunimovich, J. Tahir-Kheli, J.-K. Yu, W. A. Goddard III, and J. R. Heath, *Nature* **451,** 168 (2008).

[**332**] D. Wang, B. A. Sheriff, M. C. McAlpine, and J. R. Heath, *Nanoresearch* **1,** 9 (2008).

[**333**] J. E. Green, J. Wook Choi, A. Boukai, Y. Bunimovich, E. Johnston-Halperin, E. DeIonno, Y. Luo, B. A. Sheriff, K. Xu, Y. Shik Shin, H.-R. Tseng, J. F. Stoddart, and J. R. Heath, *Nature* **445,** 414 (2007).

[**334**] W. I. Park, G. Zheng, X. Jiang, B. Tian, and C. M. Lieber, *Nano Lett.* **8,** 3004 (2008).

[**335**] A. M. Morales and C. M. Lieber, *Science* **279,** 208 (1998).

[**336**] J. Westwater, D. P. Gosain, S. Tomiya, S. Usui, and H. Ruda, *J. Vac. Sci. & Tech., B*: **15,** 554 (197).

[**337**] Y. F. Zhang, Y. H. Tang, N. Wang, D. P. Yu, C. S. Lee, I. Bello, and S. T. Lee, *Appl. Phys. Lett.* **72,** 1835 (1998).

[**338**] D. A. Porter and K. E. Easterling, *Phase Transformations in Metals and Alloys* (Nelson Thornes, Cheltenham, UK, 1992).

[**339**] E. J. Schwalbach and P. W. Voorhees, *Nano Lett.* **8,** 3739 (2008).

[**340**] V. Schmidt, S. Senz, and U. Gosele, *Nano Lett.* **5,** 931 (2005).

[**341**] R. J. Jaccodine, *J. Electrochem. Soc.* **110,** 524 (1963).

[**342**] Y. Wu, Y. Cui, L. Huynh, C. J. Barrelet, D. C. Bell, and C. M. Lieber, *Nano Lett.* **4,** 433 (2004).

[**343**] P. Yang, *MRS Bulletin* **30,** 85 (2005).

[**344**] S. T. Lee, N. Wang, and C. S. Lee, *Mat. Sci. & Engg, B:* **A286,** 16-23 (2000).

[**345**] R.-Q. Zhang, Y. Lisfshitz, and S. T. Lee, *Adv. Mater.* **15,** 635 (2003).

[**346**] N. Wang, B. D. Yao, Y. F. Chan, and X. Y. Zhang, *Nano Lett.* **3,** 475 (2003).

[**347**] H. I. Liu, D. K. Biegelsen, F. A. Ponce, N. M. Johnson, and R. F. W. Pease, *Appl. Phys. Lett.* **64,** 1383 (1994).

[**348**] H. I. Liu, D. K. Biegelsen, N. M. Johnson, F. A. Ponce, and R. F. W. Pease, *J. Vac. Sci. & Tech., B* **11,** 2532 (1993).

[**349**] D.-B. Kao, J. P. McVittie, W. D. Nix, and K. C. Saraswat, *IEEE Trans. Elec. Dev.* **ED-35,** 25 (1988).

[**350**] R. Okada and S. Iijima, *Appl. Phys. Lett.* **58,** 1662 (1991).

[**351**] D.-B. Kao, K. C. Saraswat, J. P. McVittie, and W. D. Nix, *IEEE Trans. Elec. Dev.* **ED-32,** 2530 (1985).

[**352**] R. Juhasz, N. Elfstrom, and J. Linnros, *Nano Lett.* **5,** 275 (2005).

[**353**] A. I. Hochbaum, R. Fan, R. He, and P. Yang, *Nano Lett.* **5,** 457 (2005).

[**354**] Y. Shan, A. A. Kalkan, C.-Y. Peng, and S. J. Fonash, *Nano Lett.* **4,** 2085 (2004).

[**355**] Y. Huang, X. Duan, Q. Wei, and C. M. Lieber, *Science* **291,** 630 (2001).

[**356**] O. Englander, D. Christensen, J. Kim, L. Lin, and S. J. S. Morris, *Nano Lett.* **5,** 705 (2005).

[**357**] Y. Zhao and B. I. Yakobson, *Phys. Rev. Lett.* **91,** 035501 (2003).

[**358**] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, *Nano Lett.* **3,** 149 (2003).

[**359**] C. Ni, J. Chattopadhyay, W. E. Billups, and P. R. Bandaru, *Appl. Phys. Lett.* **93,** 243113 (2008).

[**360**] Grove A. S. Grove, *Physics and Technology of Semiconductor Devices* (John Wiley and Sons, Inc., New York, 1967).

[**361**] S. Hoffmann, I. Utke, B. Moser, J. Michler, S. H. Christiansen, V. Schmidt, S. Senz, P. Werner, U. Gosele, and C. Ballif, *Nano Lett.* **6,** 622 (2006).

[**362**] G. E. Dieter, *Mechanical Metallurgy*, 3 ed. (McGraw Hill, New York, 1986).

[**363**] R. He and P. Yang, *Nature Nanotech.* **1,** 42 (2006).

[**364**] N. Elfstrom, R. Juhasz, I. Sychugov, T. Engfeldt, A. E. Karlstrom, and J. Linnros, *Nano Lett.* **7,** 2608 (2007).

[**365**] J. A. Martinez, N. Misra, Y. Wang, P. Stroeve, C. P. Grigoropoulos, and A. Noy, *Nano Lett.* **9,** 1121 (2009).

[**366**] M. C. Lin, C. J. Chu, L. C. Tsai, H. Y. Lin, C. S. Wu, Y. P. Wu, Y. N. Wu, D. B. Shieh, Y. W. Su, and C. D. Chen, *Nano Lett.* **7,** 3656 (2007).

[**367**] R. Fan, Y. Wu, D. Li, M. Yue, A. Majumdar, and P. Yang, *J. Am. Chem. Soc.* **125,** 5254 (2003).

[**368**] R. Fan, R. Karnik, M. Yue, D. Li, A. Majumdar, and P. Yang, *Nano Lett.* **5,** 1633 (2005).

[**369**] C. R. Leao, A. Fazzio, and A. J. R. da Silva, *Nano Lett.* **7,** 1172 (2007).

[**370**] L. T. Canham, K. G. Barraclough, and D. J. Robbins, *Appl. Phys. Lett.* **51,** 1509 (1987).

[**371**] C. G. Van De Walle and J. E. Northrup, *Phys. Rev. Lett.* **70,** 1116 (1993).

[**372**] U. Gnutzmann and K. Clausecker, *Appl. Phys.* **3,** 9 (1974).

[**373**] I. Ponomareva, M. Menon, E. Richter, and A. N. Andriotis, *Phys. Rev. B* **74,** 125311 (2006).

[**374**] G. D. Sanders and Y.-C. Chang, *Appl. Phys. Lett.* **60,** 2525 (1992).

[**375**] B. Delley and E. F. Steigmeier, *Appl. Phys. Lett.* **67,** 2370 (1995).

[**376**] D. D. D. Ma, C. S. Lee, F. C. K. Au, S. Y. Tong, and S. T. Lee, *Science* **299,** 1874 (2003).

[**377**] A. J. Read, R. J. Needs, K. J. Nash, L. T. Canham, P. D. J. Calcott, and A. Qteish, *Phys. Rev. Lett.* **69,** 1232 (1992).

[**378**] Y. Cui, X. Duan, J. Hu, and C. M. Lieber, *J. Phys. Chem. B* **104,** 5213 (2000).

[**379**] S. Hoffmann, J. Bauer, C. Ronning, T. Stelzner, J. Michler, C. Ballif, V. Sivakov, and S. H. Christiansen, *Nano Lett.* **9,** 1341 (2009).

[**380**] A. Colli, A. Fasoli, C. Ronning, S. Pisana, S. Piscanec, and A. C. Ferrari, *Nano Lett.* **8,** 2188 (2008).

[**381**] C. R. Leao, A. Fazzio, and A. J. R. da Silva, *Nano Lett.* **8,** 1866 (2008).

[**382**] R. S. Muller, T. I. Kamins, and M. Chan, *Device electronics for integrated circuits*, 3 ed. (John Wiley and Sons, New York, 2003).

[**383**] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3 ed. (Wiley-Interscience, New York, 2006).

[**384**] E. Yablonovitch and T. Gmitter, *Appl. Phys. Lett.* **49,** 587 (1986).

[**385**] M. Lundstrom, *Fundamentals of Carrier Transport* (Cambridge University Press, Cambridge, UK, 2000).

[**386**] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (Wiley-Interscience, 2006).

[**387**] M. Lundstrom and J. Guo, *Nanoscale Transistors: Device physics, modeling, and simulation* (Springer, New York, 2006).

[**388**] S. D. Suk, S.-Y. Lee, S.-M. Kim, E.-J. Yon, M.-S. Kim, M. Li, C. W. Oh, K. H. Yeo, S. H. Kim, D.-S. Shin, K.-H. Lee, H. S. Park, J. N. Han, C. J. Prak, J.-B. Park, D.-W. Kim, D. Park, and B.-I. Ryu, *IEEE Trans. Nanotech.* **7,** 181 (2008).

[**389**] W. M. Weber, L. Geelhaar, A. P. Graham, E. Unger, G. S. Duesberg, M. Liebau, W. Pamler, C. Cheze, H. Riechert, P. Lugli, and F. Kreupl, *Nano Lett.* **6,** 2660 (2006).

[**390**] M.-V. Fernandez-Serra, C. Adessi, and X. Blase, *Nano Lett.* **6,** 2674 (2006).

[**391**] S. Datta, *Electronic Transport in Mesoscopic Systems* (Cambridge University Press, New York, NY, 1995).

[**392**] A. Kikuchi, *Phys. Stat. Sol. A* **175,** 623 (1999).

[**393**] H. Schmid, M. T. Bjork, J. Knoch, S. Karg, H. Riel, and W. Riess, *Nano Lett.* **9,** 173 (2009).

[**394**] K. Kobayashi, *Phys. Rev. B* **69,** 115338 (2004).

[**395**] M. Fox, *Optical properties of solids* (Oxford University Press, New York, NY, 2001).

[**396**] D. M. Lyons, K. M. Ryan, M. A. Morris, and J. D. Holmes, *Nano Lett.* **2,** 811 (2002).

[**397**] S. S. Iyer and Y.-H. Xie, in *Porous Silicon*, edited by Z. C. Feng and R. Tsu (World Scientific, River Edge, NJ, 1994).

[**398**] T. Westover, R. Jones, J. Y. Huang, G. Wang, E. Lai, and A. A. Talin, *Nano Lett.,* **9,** 257 (2009).

[**399**] B. M. Kayes, N. S. Lewis, and H. A. Atwater, *J. Appl. Phys.* **97,** 114302 (2005).

[**400**] J. Nelson, *The Physics of Solar Cells* (Imperial College Press, London, UK, 2003).

[**401**] W. Shockley and H. J. Queisser, *J. Appl. Phys.* **32,** 510 (1961).

[**402**] G. Goncher and R. Solanki, in *Semiconductor nanowire photovoltaics*, 2008 (SPIE), p. 70470L-1.

[403] A. Goetzberger, C. Hebling, and H.-W. Schock, *Mater. Sci, & Engg. R* **40,** 1-46 (2003).

[404] L. Tsakalakos, J. Balch, J. Fronheiser, M. Y. Shih, S. F. LeBoeuf, M. Pietrzykowski, P. J. Codella, B. A. Korevaar, O. V. Sulima, J. Rand, A. Davuluru, and U. Rapol, *J. Nanophotonics* **1,** 013552-10 (2007).

[405] E. Yablonovitch and G. D. Cody, *IEEE Trans. Elect. Dev.* **ED-29,** 300 (1982).

[406] K. Peng, Y. Xu, Y. Wu, Y. Yan, S.-T. Lee, and J. Zhu, *Small* **1,** 1062 (2005).

[407] R. A. Street, P. Qi, R. Lujan, and W. S. Wong, *Appl. Phys. Lett.* **93,** 163109 (2008).

[408] T. Stelzner, M. Pietsch, G. Andra, F. Falk, E. Ose, and S. Christiansen, *Nanotechnology* **19,** 295203 (2008).

[409] M. Zervos, *Semicond. Sci. & Tech.* **23,** 075016 (2008).

[410] T. J. Kempa, B. Tian, D. R. Kim, J. Hu, X. Zheng, and C. M. Lieber, *Nano Lett.* **8,** 3456 (2008).

[411] F. Leonard and J. Tersoff, *Phys. Rev. Lett.,* **83,** 5174 (1999).

[412] B. Tian, X. Zheng, T. J. Kempa, Y. Fang, N. Yu, G. Yu, J. Huang, and C. M. Lieber, *Nature* **449,** 885 (2007).

[413] M. D. Kelzenberg, D. B. Turner-Evans, B. M. Kayes, M. A. Filler, M. C. Putnam, N. S. Lewis, and H. A. Atwater, *Nano Lett.* **8,** 710 (2008).

[414] T. M. Rumke, J. A. Sanchez-Gil, O. L. Muskens, M. T. Borgstrom, E. P. A. M. Bakkers, and J. Gomez Rivas, *Opt. Exp*.**,** 5013 (2008).

[415] O. L. Muskens, J. G. Rivas, R. E. Algra, E. P. A. M. Bakkers, and A. Lagendjik, *Nano Lett.* **8,** 2638 (2008).

[416] J. Zhu, Z. Yu, G. F. Burkhard, C.-M. Hsu, S. T. Connor, Y. Xu, Q. Wang, M. McGehee, S. Fan, and Y. Cui, *Nano Lett.* **9,** 279 (2009).

[417] S.-H. Yang, M. L. Cooper, P. R. Bandaru, and S. Mookherjea, *Opt. Exp.,* **16,** 8306 (2008).

[418] X. L. Feng, R. He, P. Yang, and M. L. Roukes, *Nano Lett.* **7,** 1953 (2007).

[419] R. He, X. L. Feng, M. L. Roukes, and P. Yang, *Nano Lett.* **8,** 1756 (2008).